National Aeronautics and Space Administration

EEE Parts Bulletin

Electrical, Electronic, and Electromechanical

A periodic newsletter of the NASA Electronic Parts Program / NASA EEE Parts Assurance Group and the Jet Propulsion Laboratory

August 2016–May 2017 • Volume 9, Issue 1 (Published since 2009), June 16, 2017

Second Special Edition on Electrostatic Discharge (ESD)

Damage from ESD is a major cost to the microcircuit industry in terms of time, money, and mission risk. The first issue dealt with the need to upgrade specifications related to ESD and suggestions for better ESD practices wherever parts are manufactured, stored, or prepared for shipment. This second ESD special issue focuses on a parts failure investigation that ultimately concluded that ESD was the most likely cause of the failure. The issue also includes an important reminder about regular ESD testing and a table of standard microcircuit drawings that were recently reviewed,

Figure 1 is an example of damage that was probably caused by ESD.

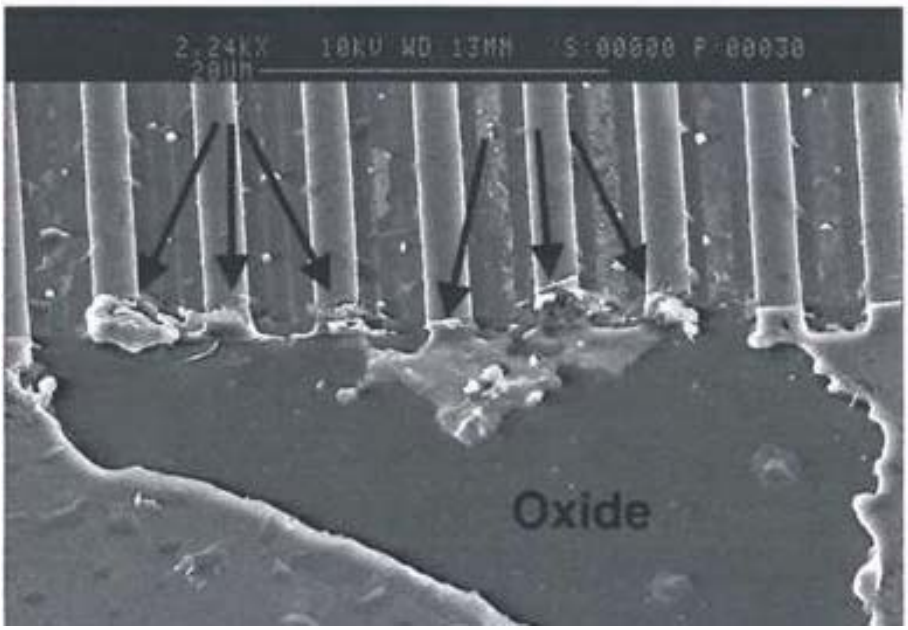

Fig. 1. Detailed view of a damaged site on a metal oxide semiconductor field-effect transistor (MOSFET) probably caused by ESD.

ESD, the Silent Killer—

A. Background

There are several great points to consider with respect to ESD knowledge, practice, and compliance. However, the key for ESD program success is consistency. If we detect the results of an event, then, we [the operational group] should be able to ascertain and confirm that we never have any lapses in the program implementation. With systematic practices, we should be able to surmise that there is no way any events can occur on the organizational project watch.

ESD is the silent killer in electronics, and the resulting impacts are hidden project costs that are the motivator to address project risk cost and schedule impacts. When an ESD event occurs, one of three scenarios may play out.

1) There is no impact, and no detrimental result.
2) There is a catastrophic strike and the immediate electronics operation failure is detected, isolated, and repaired. Repairs may be easy or done at great expense, but they are done.

3) The most undesirable event may happen. Undetected damage to one or more parts results in latent defects that are either detected during ground test operations or (worse yet) during mission operations (when any resulting failures may be beyond repair).

The later an ESD event happens in the product life cycle of the system, the greater the project cost for repair. Latent defect end-of-life prediction is weak due to lack of access to flight and in-orbit malfunctioning hardware for analysis purposes.

Under these circumstances, we need the highest possible confidence levels in our ESD program compliance at all times in order to be fully effective.

Part replacement costs not only include part costs, which can range from about $100 (for a typical active part) to about $40,000 (for field-programmable gate arrays, FPGAs), but also the repair labor and mission assurance logistics and disposition. The real hidden costs can potentially escalate when considering the diligence to complete “run to ground” root cause failure analysis, possibly numerous technical/material review boards and completion of all final documentation for disposition of the ESD failure event.

The cost of the labor hours alone associated with all the program/project technical authorities, subject matter experts, and electronics-hardware assembly personnel attending the disposition meetings can in most cases out cost the replacement value of the damaged part alone. Many of these personnel also participate in system teardown, acquisition of the new part screening/testing of the new part, emplacement of the new part, reassembly, and retesting of the repaired system. Therefore, prevention is a multi-faceted reward.

B. Examples

Below are a few examples of some metallic oxide semiconductor field-effect transistor (MOSFET) devices that were damaged during the assembly of a recent space flight International Space Station (ISS) support instrument box. The parts were received, in ESD protective packaging and not removed until board-level assembly soldering took place. The failed board-assembly-level verification and the ensuing troubleshooting ruled out design or operational issues. The suspect parts were removed, tested, and shipped off for failure analysis.

Figure 2 shows the PCB assembly with two noted nonfunctional parts circled in red. Although not conclusive, the corner location of damaged parts on the board was thought to be important to the forensics analysis. One theory implied that handling of the board (by the perimeter) allowed for the ESD event to contact these parts directly. During transport, the board is handled only inside an ESD-approved materials bag. There were questions as to the integrity of these transport bags. Due to bag traceability and reuse issues, there was no definite conclusion on this concern.

Figures 3 thru Figure 7 Show the die and damage areas from various photographic and radiographic perspectives. During upper-level assembly circuit troubleshooting, the potential for design or operational damaging voltages to the MOSFET gates were conclusively ruled out. The circuit was incapable of generating the necessary damaging voltages that would have the effect observed.

C. Investigation Conclusion

The conclusion of this ESD failure investigation was that failure was attributed to user error but review of all ESD compliance logs showed that all precautions were taken during operator handling. Due to lack of further evidence, the OCM and the PCB assembly operation were not ruled out as possible culprits, but neither could be confirmed.

Under these circumstances the team was advised of the event and warned of the total cost for repair and the need to double check all future handling procedures. The board was repaired with same lot date code parts, and there were never any repeat operational issues with that PCB assembly nor at the box operational level. The “Silent Killer” only struck once on that program. At least as far as can be determined at this time.

Figures 1 through 7 (provided courtesy of NASA Langley Research Center) were generated by Hi-Rel Labs as part of a project Component Failure Investigation at Langley.

For more information, contact

John E. Pandolf 757 864-9624

Fig. 2. Damaged parts are circled in red.

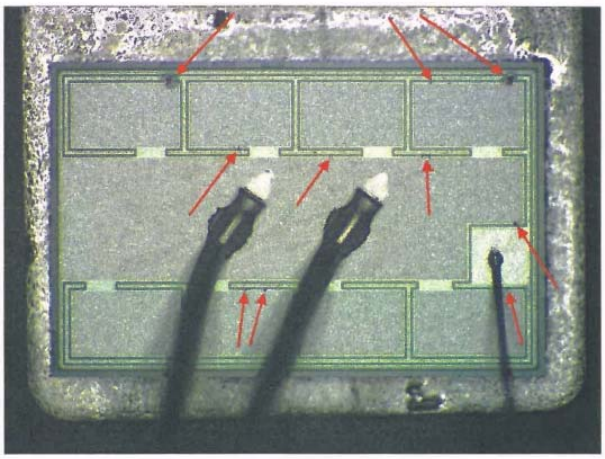

Fig. 3. Optical micrograph of the die in the failed device. The red arrows indicate the damage sites.

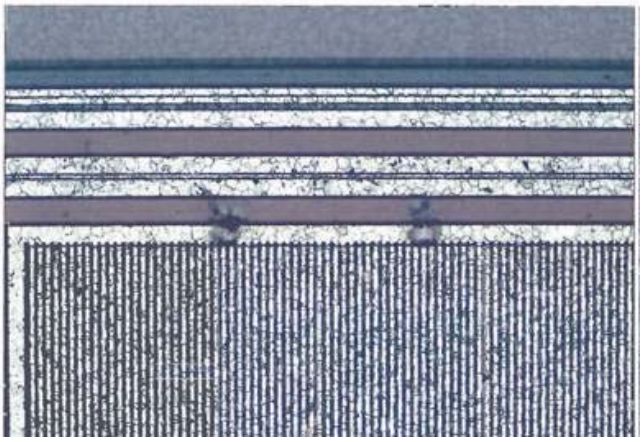

Fig. 4. Detailed view of the damage sites on the die.

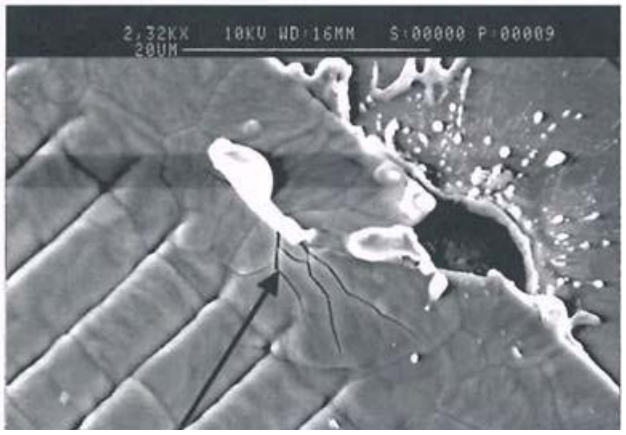

Fig. 5. SEM image of one of the damage sites. The arrow indicates the area where the damage originated

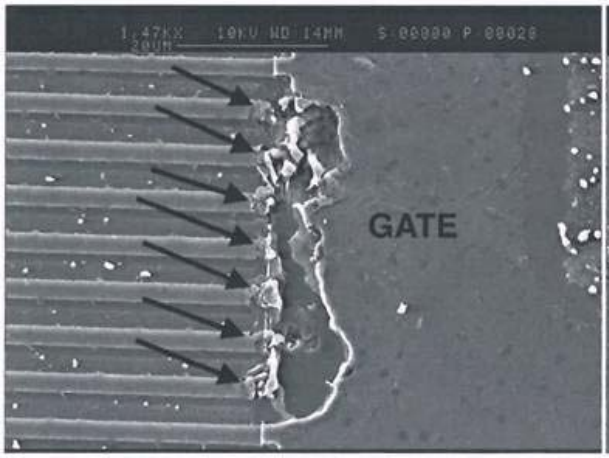

Fig. 6. SEM image of the FET after delayering. The arrows indicate the damage at the ends of the gate runners.

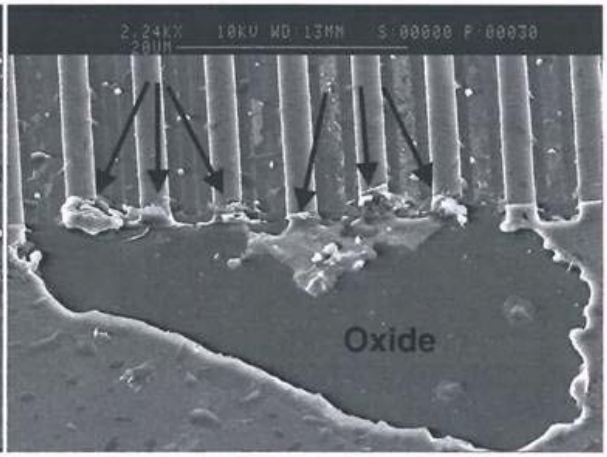

Fig. 7. SEM image of another damaged area on the die. Note that the gate polysilicon fused during the failure, which is why the oxide is visible.

A Reminder That Details Are Crucial for ESD—Example, Heel Straps

Over the course of many years, NEC Corporation of America has conducted audits of a variety of manufacturers handling ESD-sensitive materials, and have seen many issues regarding ESD handling. Many of them are small mundane details; yet, failing to maintain the discipline in performing them can lead to expensive ESD parts incidents.

One type of recurring problem we have seen many times is the misuse of ESD heel strap testers where the testing is conducted with ESD flooring installed. The grounding straps must be periodically testing to be sure their function has not been compromised by being stepped on, being caught in doors, etc.

For operators wearing heel straps or conductive footwear on both feet, the proper use would be to place the foot-under-test on the test plate, raise the untested foot from the floor and to depress the test button of the tester. Then, the raised foot is switched to test the grounding of the other foot strap.

It is obvious, it is a standard procedure, but it is easily forgotten. Audits have uncovered usage where the operator leaves the untested foot on the floor, allowing a conductive path to the floor even if one of the straps is not functional, distorting the test results.

Lesson: Go through the tests by the procedures book rather than, "I remember it all." Forgetting little details can cause big sparks.

For more information, contact

Robin Gomi, NEC Corporation of America

978-758-3703

New Standard Space Microcircuits for Potential Use on Flight Projects

NASA is in the review and approval cycle of new space monolithic (Class V) and hybrid (Class K) microcircuits. Many of these products are guaranteed to be radiation hardened to the levels specified in the Standard Microcircuit Drawings (SMDs). Table 1 lists the space product SMDs approved in FY2017 until June. Radiation-hardened parts are denoted by (rad)" and non-radiation-hardened by "(nonrad)". The microcircuit manufacturers have reported strong demand for space products so far in 2017. This will provide more options to the designers of NASA flight hardware.

Table 1. FY2016 and FY2017 Released SMDs as of March 20, 2017.

SMD No.	Function	Manufacturer
5962-11229	Dual Pos & Neg Regulator (rad)	Anaren Microwave Inc.
5962-15217	DC/DC Converter (rad)	VPT Inc.
5962-15218	DC/DC Converter (rad)	VPT Inc.
5962-13201	14-bit DAC (rad)	Aeroflex
5962-14205	Instrumentation Amplifier (rad)	ADI (AD8229)
5962-14216	DC-DC Converter (rad)	Crane Electronics
5962-14221	Precision Voltage Reference and Thermometer (rad)	Aeroflex
5962-14231	Analog-to-Digital Converter (rad)	TI (ADS1282)
5962-15211	Analog-to-Digital Converter (rad)	ADI (AD9643)
5962-15224	DC-DC Converter (non-rad)	International Rectifier
5962-15236	Operational Amplifier (rad)	ADI (AD4084)
5962-15239	Configurable Logic Gates (rad)	Aeroflex (UT54ACS2S99S)
5962-15244	High-Speed CMOS 8-bit Bus Switch (rad)	Aeroflex CO Springs
5962-15245	High-Speed CMOS 20-bit Bus Switch (rad)	Aeroflex CO Springs
5962-16201	Quad Precision Amplifier (nonrad)	Anaren Microwave Inc.
5962-16202	DC-DC Converter (non-rad)	VPT
5962-16203	DC-DC Converter (non-rad)	VPT
5962-16204	Op-Amp (rad)	ST Micro (RHR61)
5962-16205	Quad op-amp (rad)	ST Micro (RHR64)
5962-16210	Octal Diode Array Pairs with redundancy (nonrad)	Microsemi SOC
5962-89981	Linear Positive Regulator (rad)	Linear Technology Corp.
5962-99560	MOSFET Driver (rad)	STM (PM4424)

For more information, contact

Shri Agarwal 818-354-5598

Resistors and Electrostatic Discharge (ESD) Susceptibility

MIL-PRF-55342 resistors are the primary NASA standard for established reliability chip resistors. These resistors are used in a wide variety of mission-critical applications, and will be the main focus of this article. Current knowledge is that passive components such as resistors can sometimes be more sensitive to ESD than active components, which were historically considered at-risk.

Resistors are a technology area where there is a pronounced trade-off of greater capability vs. greater sensitivity. There is no designator for thin film versus thick in the part number, just a temperature coefficient (TCR). Thin films have a low TCR, whereas thick films have higher TCRs. Thin film resistors are much more ESD sensitive than thick films. Thin films can be sold against requirements for all TCR values so all part numbers are assumed to be ESD sensitive even though most high TCR lots are likely to be thick film and quite ESD resistant. ESD precautions should be taken when handling these devices. Field failures of thin-film resistors, in particular, have been attributed to ESD events and have resulted in anything from a few percent deltas in resistance to full open circuit failure.

Per MIL-PRF-55342, Section 6.6: "Under relatively low humidity conditions, some types of film resistors, particularly those with small dimensions and high sheet resistivity materials, are prone to sudden significant changes in resistance (usually reductions in value) and to changes in temperature coefficient of resistance as a result of discharge of static charges built up on associated objects during handling, packaging, or shipment."

One Manufacturer's Approach to ESD Mitigation and Control

State of the Art, Inc. (SotA) is one of DLA's Qualified Parts List (QPL) resistor manufacturers. The following material describes the SotA approach to mitigating and controlling ESD. However, it must be emphasized that ESD practices vary significantly among manufacturers and users. Thus, the ESD practices of other resistor manufacturers may be different from those of SotA.

Table 1 shows SotA thick- and thin-film resistors tested in accordance with MIL-STD-883, Method 3015. ESD sensitivity depends on the manufacturing technology, the case length, and the resistance value.

The MIL-specifications SotA uses to address the sensitivity of resistors to ESD events are as follows.

MIL-STD-1686 addresses ESD control programs and SotA's full classification of parts, assemblies, and equipment is accomplished by using three defined models

- Human body model (HBM)
- Machine model (MM (there is some discussion over whether machine model is still applicable)
- Charged device model (CDM)

MIL-HDBK-263 is the ESD control handbook that addresses ESD considerations for specific components and assemblies and classifies devices as class 1, 2, or 3 (HBM classes) in accordance with MIL-STD-1686. It refers to the HBM test method, MIL-STD-883, method 3015, as the "…the military ESD test method for microelectronics."

ANSI/ESDA-JEDEC JS-001-2010 and **MIL-STD-883H**, method 3015.8 define the component's ability to withstand ESD sensitivity classes (Table 2) and the cases matched to sensitivity classes for thin- and thick-film resistors.

Table 2. SotA Resistor ESD Sensitivity Classification.

SotA Resistor Technology	Resistor Chip Size	ESD Classification per MIL-STD-1686 (HBM)	ESD Voltage Threshold
Thin Film	0402 and 0505	1C	<2000 V
	0302, 0502, 0603, and 0705	2	<4000 V
	1005, 1010, 1206, 1505, & 2208	3A	<8000 V
	2010 & 2512	3B	≥8000 V
Thick Film	0302 & 0402	1B	<1000 V
	0502, 0505 0603, 0705, & 1206	1C	<2000 V
	1005 & 1505	2	<4000 V
	1010	3A	<8000 V
	2010, 2208, & 2512	3B	≥8000 V

*NOTE: This table and many of the citations herein have been sourced directly from SotA and its publications. It is recommended you contact your resistor manufacturer for comparable data packs and any relevant ESD precautions.

We thank State of the Art, Inc. for their willingness to share their information and approaches regarding film resistor device history and ESD test procedures used with these devices.

Typical Types of ESD Damage Recorded by NASA

According to the NASA Goddard Space Flight Center, testing has shown that imposed ESD damage produces four basic effects: Little or no damage, current crowding, internal arcing, and external arcing. They reported it was rare to see all of these effects in the same test network. The following images show ESD damage to resistive film layers (see Figures 8–11) [1].

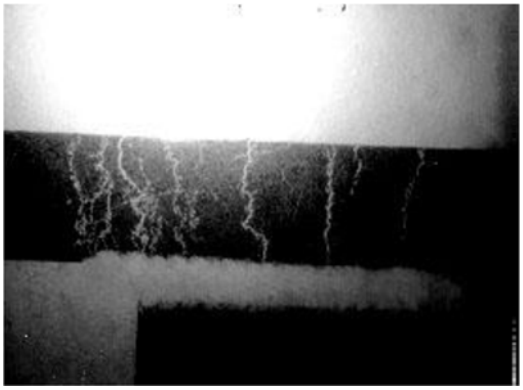

Fig. 8. Vicinal view of ESD induced damage to a thin-film resistor network chip during ground testing [1].

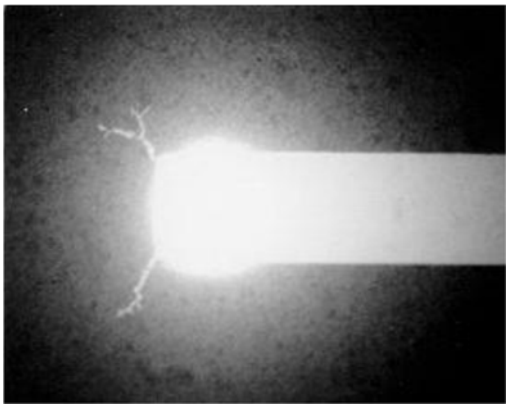

Fig. 9. Vicinal illumination view of corner crowding induced damage [1].

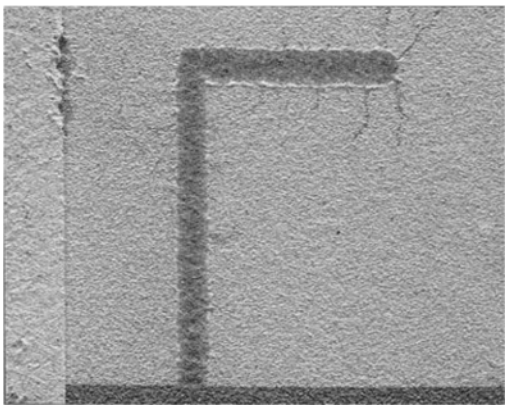

Fig. 10. SEM view of ESD damage in a tantalum nitride resistor. Note the internal arcing damage to the left of the laser kerf [1].

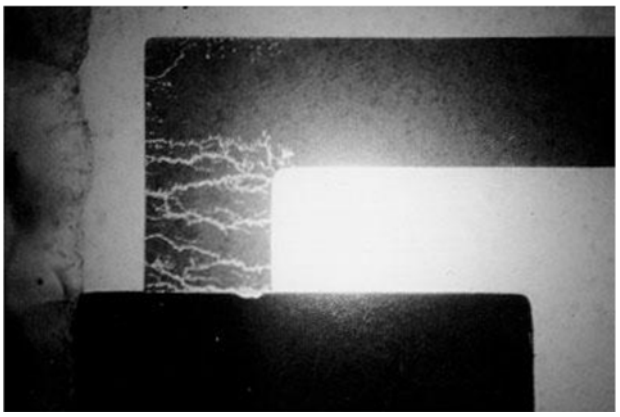

Fig. 11. Vicinal illumination view of transverse cracking typical of relatively high voltage ESD damage [1].

References

1) ***Electrostatic-Discharge (ESD) Failures in Thin-Film Resistors***, Scott M. Hull, NASA Goddard Space Flight Center, Greenbelt, MD, Jan. 1, 1999. https://ntrs.nasa.gov/search

2**) MIL-PRF-55342**, *Resistor, Chip, Fixed, Film, Nonestablished Reliability, Established Reliability, Space Level, General Specification For*, Rev. H, U.S. Department of Defense, Jan. 29, 2016 https://landandmaritimeapps.dla.mil/Downloads/MilSpec/Docs/MIL-PRF-55342/prf55342.pdf

3) **MIL-HDBK-263**, *Electrostatic Discharge Control Handbook for Protection of Electrical and Electronic Parts, Assemblies and Equipment (Excluding Electrically Initiated Explosive Devices) (Metric)*, Rev. B, July 31, 1994.

4) **MIL-STD-883H, Method 3015.8**, Test Method Standard, Microcircuits, Rev. K, Change 2, ***Test Method 3015, "Electrostatic Discharge Sensitivity [ESDS] Classification,"*** U.S. Department of Defense, July 20, 2016.

https://landandmaritimeapps.dla.mil/Programs/MilSpec/ListDocs.aspx?BasicDoc=MIL-STD-883

5) **MIL-STD-1686**, *Electrostatic Discharge Control Program for Protection of Electrical and Electronic Parts*, Assemblies and Equipment (Excluding Electrically Initiated Explosive Devices), Rev. C, U.S. Department of Defense, Oct. 25, 1995.

6) **ANSI/ESDA-JEDEC JS-001-2010**, *Electrostatic Discharge Sensitivity Testing -- Human Body Model*, ESD Association & JEDEC Solid State Technology Association, Jan. 13, 2010. https://webstore.ansi.org/

7) **State of the Art, Inc. Catalog. CAT# 1628**. http://www.resistor.com

For more information, contact

Jennifer Hill, 818- 354-3290

Class Y Qualification / Certification Status

New devices, such as the Xilinx Virtex-4 and -5 FPGAs (ceramic-based flip-chip non-hermetic construction) have been of great interest to space hardware designers. They represented advances in packaging, smaller feature sizes (65 nm–90 nm), e.g., flip-chips and column-grid arrays.

But, it didn't fit any of the existing categories. Therefore, NASA worked with the space community to develop a new Class Y. The processes that finally accomplished this infusion of new technology into the QML system are summarized in Figure 12.

As of June 2017, the suppliers certified and qualified for class Y were as shown below.

Class Y SMD

DLA generated the first SMD draft for a QMLY application specific integrated circuit (ASIC).

Qualified Manufacturer

- Honeywell, Plymouth, MN

Certified Manufacturers

- *Cobham, Colorado Springs, CO*
- *Honeywell, Plymouth, MN*

Certified Assembly and Test

- Kyocera, San Diego, CA

Certified Column-Attach Manufacturing

- Six Sigma, Milpitas, CA
- Micross, Crewe, UK
- BAE Systems, Manassas, VA

Recommendation

- Develop slash sheets for BME (Base Metal Electrode) IDCs (Inter-Digitized Capacitors) as soon as possible.

Note:

- Certification is demonstration of capability to produce a part.
- Qualification is actually producing the part per the space requirements.

For more information, contact

Shri Agarwal 818-354-5598

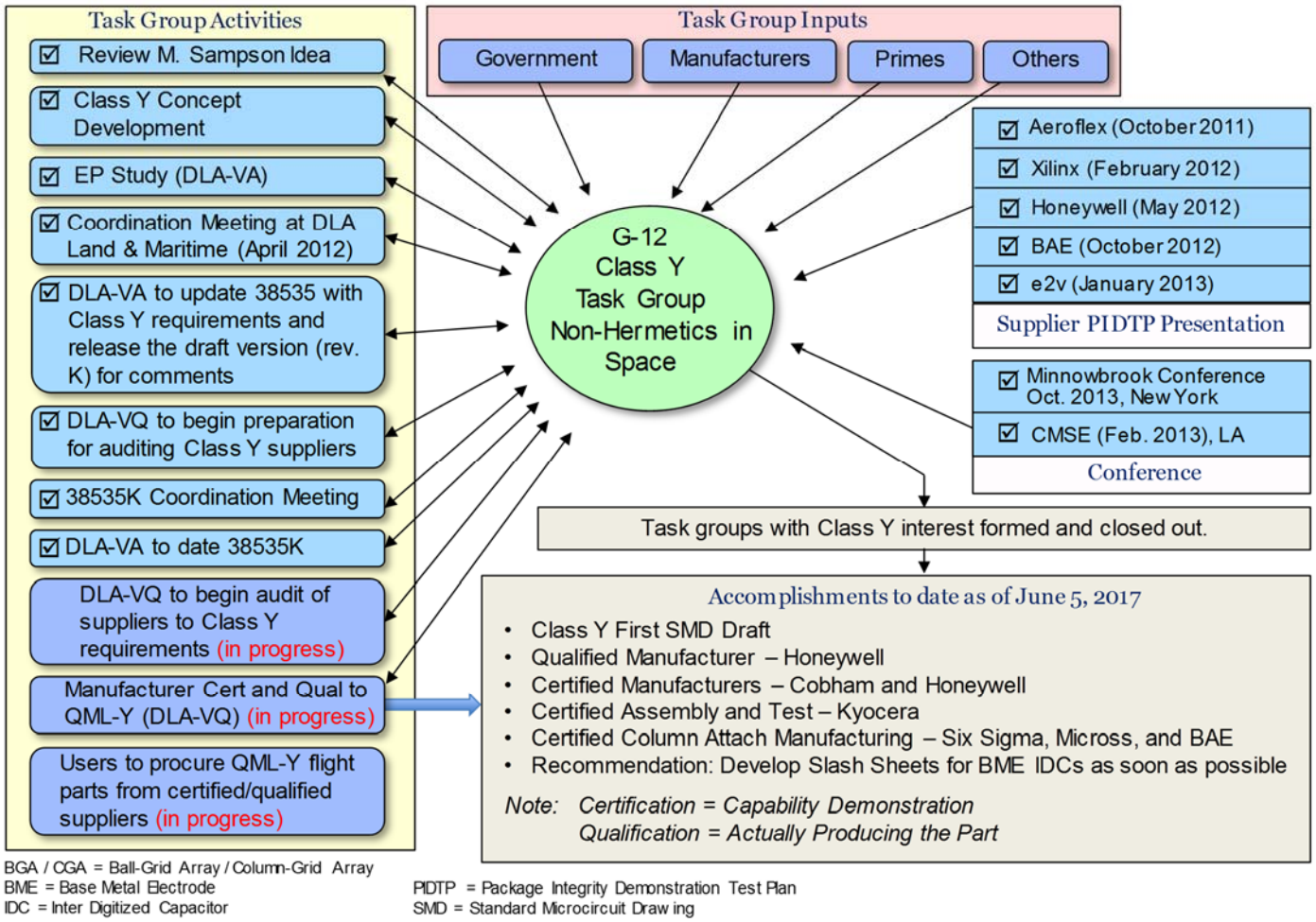

Fig. 12. Infusion of the New Class (Y) Technology into the QML System for Space.

NASA Parts Specialists Recent Support for DLA Land and Maritime Audits performed at:

- DDC (formerly Maxwell), San Diego, CA
- Delta Electronics Inc., Taoyuan Shien, TW
- Honeywell Aerospace, Plymouth, MN
- Microsemi-Philippines, Laguna PH
- MSK Products (Anaren, Inc.), East Syracuse, NY
- Tong Hsing, Laguna, PH

Upcoming Meetings

- 8th Annual Electronics Technology Workshop (ETW), Greenbelt, MD, June 26–29, 2017
- IEEE Nuclear and Space Radiation Effects Conf. (NSREC 2017), New Orleans, LA, July 17–21, 2017
- JEDEC/SSTC G-11 & G-12 meeting, Columbus, OH, Sept. 11–14, 2017

Contacts

NEPP https://nepp.nasa.gov/

Michael J. Sampson 301-614-6233
michael.j.sampson@nasa.gov

Kenneth A. LaBel 301-286-9936
kenneth.a.label@nasa.gov

NEPAG (within JPL)
http://atpo.jpl.nasa.gov/nepag/index.html

Shri Agarwal 818-354-5598
Shri.g.agarwal@jpl.nasa.gov

Roger Carlson 818-354-2295
Roger.v.carlson@jpl.nasa.gov

ATPO http://atpo.jpl.nasa.gov
Doug Sheldon 818-393-5113
Douglas.J.Sheldon@jpl.nasa.gov

JPL Electronic Parts http://parts.jpl.nasa.gov
Mohammad M. Mojarradi 818-354-0997
Mohammad.M.Mojarradi@jpl.nasa.gov
Jeremy L. Bonnell 818-354-2083
Jeremy.L.Bonnell@jpl.nasa.gov

Previous Issues:
Other NASA centers:
http://nepp.nasa.gov/index.cfm/12753

Public Link (best with Internet Explorer):
https://trs.jpl.nasa.gov/discover?query=eee+parts+bulletin

www.nasa.gov
National Aeronautics and Space Administration

Jet Propulsion Laboratory
California Institute of Technology
Pasadena, California