DFT is so Beautiful - Why does it stand so Isolated?

“Design for Test” or “Design for Testability” (DFT) is often a uniquely perceptive endeavor when performed during the Design Development activity. Those organizations that have embraced the DFT activity as a fundamental design competency, have gained a growing appreciation for the value it provides. As design complexity continues to increase, the broader use of DFT will become more ubiquitously recognized as an integral piece of the Design Development process. DFT’s role has been a key factor in industry’s greatly improved production test and fault isolation capabilities over the past few decades while providing dividends of confidence to producers in the form of added product quality at the expectation of improved customer satisfaction. If this holds true, then the beauty of improved customer satisfaction lies in the promise of potentially continued and increasing longer term sales. Beauty attracting more beauty.

Where Are We Now?

But in the traditional application of DFT, unfortunately, the sense of value and beauty, prematurely fails to endure. The value of traditional DFT is soon discovered to be too narrowly realized when considering complex hardware design domains outside its abrupt island coastal borders of digital or software-enabled, electronic design. How can that be so – We often hear that DFT is effective at the “system level”? What are we missing? At this point, we need to determine what is universally understood to be the “system level”. Here is where we gather our first symptom of one of the primary root causes for industry’s lack of awareness of its role in the broader realization of such enduring DFT beauty.

A Brief Look Back:

Ralph A. DePaul, Jr. pioneered methods and tools to facilitate a consistent and exhaustive approach to full System Level "Testability", beginning in the 1960's. In 1965, Mr. DePaul prepared a document ("Design Disclosure Format Document") that would ultimately be incorporated into the MIL-M-24100B, the precursor to MIL-STD 2165.

Lawson Discusses Value of Logistics Plans

The role of logistics in business planning was discussed by Aeronutronic General Manager John B. Lawson at a re-cent dinner meeting of the Society of Logistics Engineers.

"It is surprising," Lawson said in opening, "that your organization was founded onlv about three years ago, when in reality your profession has been in existence for many centuries. "

He said that although industry was concerned in the past with logistics, it operated in a "hit or miss" fashion.

"However, in recent years there has been an increased recognition that logistics is a necessary business investment," Lawson said. "In developing and producing a new system, proper attention must be given to how it will he used and serviced. Otherwise, a highly successful and economical system could be subject to malfunction, increased operating costs and premature obsolescence.

"It is for this reason that we must plan the logistics requirement from the time we receive a development contract through the production phase and throughout the system's operational life."

Lawson was introduced by Ralph De Paul, manager of the Logistics and Field Service Department. Ordnance and Electromechanical Operation.

"There is no question that a company's logistic efforts must be accomplished well to achieve customer satisfaction and repeat business," De Paul said.

"Studies show that in the Department of Defense, about 25 per cent of the total costs in the life cycle of a program goes for logistics. This fact, coupled with the profit potential of this type of effort, provides a strong incentive to support our equipment while in service.

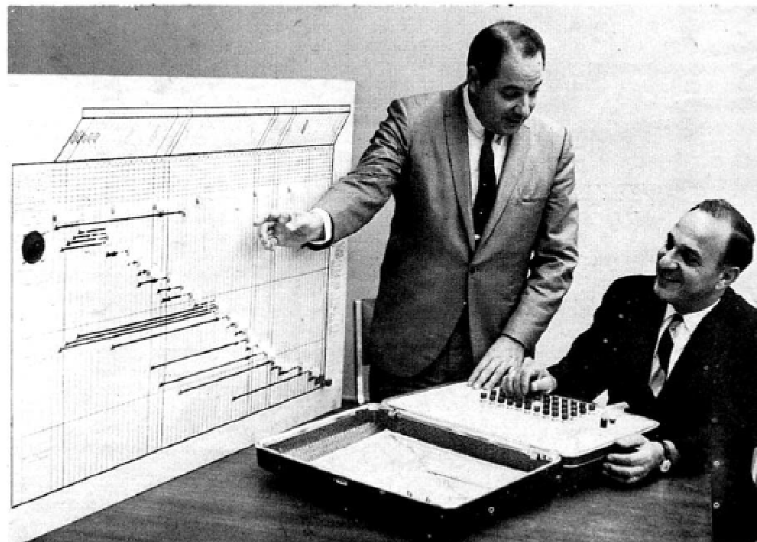
"One way that we have contributed significantly to the maintenance of equipment is the development of the logic model approach." De Paul said. "This technique has enabled us to provide mathematical models in the form of symbolic illustrations to our Chaparral and XM I40 customers that permit a technician or mechanic to isolate and repair malfunctions of equipment easier, faster and with considerably less documentation than previous systems."

The logic model for the XMI40 gun was featured at the meeting. It detailed, in logical order, the entire sequence of operation of the gun.

The model was constructed by Carl Spitzer and Gus Daskalakis under De Paul's direction. De Paul previously had worked out a similar scheme for the Chaparral weapon system.

He explained that these first logic models were prepared manually. but that the Scientific Programming Department has developed a program which permits the charts to he prepared and changed by the computer, with significant cost savings.

"Not too far in the future," De Paul said, "the logic model approach will permit imagery devices to be used in conjunction with a computer to diagnose malfunctions as they occur, provide 'hard copy' readout of several logistic parameters affected by singular, multiple and cumulative malfunctions, and issue instructions to correct deficiencies."



LOGIC MODEL — Ralph De Paul (standing) and Gus Daskalakis display logic model for the XM140 gun, which assists in equipment maintenance. A model also has been constructed for Chaparral weapon system.

April, 1969 7

After more than a decade of proving the feasibility and value of "Testability Design" before all branches of the US Armed Services, Mr. DePaul sought the assistance of a local US Congressman to secure the recognition of "Testability" as a necessary component of the Design Development activity for complex US military systems. This arduous process was preceded by Mr. DePaul's relentless pursuit and successful performance of dozens of small-to-medium sized direct contracts with each agency within the US DoD. Most of the awarded contracts were performed during a rapidly changing point in time that witnessed the advancement in electronics and the violent evolution of software forms vying for footholds in society during the uncertainty caused by these dynamics. Regardless of many challenges, Mr. DePaul proved applicability and success on a wide variety of complex military systems during that time. Eventually, in working with Mr. William L. Keiner (author of MIL-STD 2165 "Testability") and in coordination with the US Joint Logistics Command, Mr. DePaul and DSI were finally successful in establishing the basis for testability as a design development activity. This journey culminated in the 1986 release of MIL-STD-2165.

JOHN SLATTERY
PROFESSIONAL ACHIEVEMENT AWARD

:

The late Ralph DePaul, Jr. is the 1994 recipient of the **John Slattery Professional Achievement Award.** It will be presented to a member of his family at the AUTOTESTCON awards luncheon for his contributions to automatic testing in support of the United States national security posture. Mr. DePaul founded DETEX Systems, Inc., known for STAT, a widely used testability analyzer and for opening new pathways for "model based diagnostics.

The award, sponsored by the Automatic Testing Committee of the National Security Industrial Association (NSIA-ATC), honors the memory of John Slattery, a software engineer with the General Dynamics Electronics Division who contributed to the enhancement of automatic test equipment in military and industrial applications. He was active in AUTOTESTCON, the NSIA's Automatic Testing Committee and the Modular Automatic Test Equipment (MATE) Users' Group (MUG) and was Chairman of the group's Subcommittee for Control and Software.

Mr. DePaul was active in the support community from 1956 when he joined Hughes Aircraft Company in Fullerton, CA until his death in 1993. At Hughes, he assisted in the hardware design of nine fi'e control systems and one air weapons control system for the U.S. Air Force, and designed the memory assembly for the MA-1 Flight Control System. He performed all levels of testing on systems he helped design plus the fi'st Frequency Scan Radars used in the Army and Navy, the FALCON Missile System for the Air Force and the TOW Guided Missile System for the Army. It was during this period he began research and concept development of what today is Functional Dependency Modeling. In 1960, he became manager of Hughes' Integrated Logistics and served in that capacity until joining Ford Aerospace five years later as manager of Integrated Logistic Support. There, he continued his work on Function Dependency Model by satisfying maintainability demonstration requirements for a series of weapons systems and developed a forerunner to a portable computerized maintenance aid.

Mr. DePaul formed DETEX Systems in 1975 and was a leading advocate of testability before the U.S. Congress and the NSIA and JPL subcommittees on testing. His persistence led to recognition of a need for a military standard on testability which resulted in ML-STD-2165. At DETEX, he dealt with all types of electronic (analog and digital), mechanical, optic and electro-mechanical hardware.

He earned a MS degree in physics and mathematics from UCLA and a BS degree in physics and mathematics from Loyola University, Chicago.

Previous winners of the John Slattery Award:

1987 - A. Padget Peterson
1988 - Mary Kaye Allen
1989 - George A. Emilio
1990 - J.A. (Bert) Houston
1991 - Vic Bloom
1992 - George W. Neumann
1993 - James W. Smith

"Mr. DePaul formed DETEX Systems, Inc. in 1975 and was a leading advocate of testability before the U.S. Congress and the NSIA and JPL subcommittees on testing. His persistence led to the recognition of a need for a military standard on testability which resulted in MIL-STD-2165".

DIAGONOSABLITY CHARACTERISTICS AND METRICS

IEEE Std 1522-2004

Annex A

(informative)

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[B1] DePaul, R. A. Jr., "Logic modeling as a tool for testability," *Proceedings of the IEEE AUTOTESTCON*. New York: IEEE Press, 1985, pp. 203–207.

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[B3] Gould, E., and Hartop, D., "Thinking beyond the group size fetish: Towards a new testability," *Proceedings of the IEEE AUTOTESTCON*. New York: IEEE Press, 1999, pp. 673–684.

[B4] IEEE 100, The Authoritative Dictionary of IEEE Standards Terms.[6]

[B5] Keiner, W., "A Navy approach to integrated diagnostics," *Proceedings of the IEEE AUTOTESTCON*. New York: IEEE Press, 1990, pp. 443–450.

The Annex A of IEEE Std 1522-2004 (Testability and Diagnosability Characteristics and Metrics) identifies DSI's (Mr. DePaul, Mr. Gould & Mr. Hartop) earlier contribution to this document (B1, B2 & B3). Author of Testability, MIL-STD-2165, Keiner, W. is also identified (B5) at the beginning of this Annex.

The Two (2) "Testability's"

Over the last couple decades, the understanding of designing for "System Testability" split into two schools – diverging from its origin where "system" had been understood to be the fully fielded vehicle or equipment – to today's more popular understanding of the discipline of "Testability" as being more focused on "Designing For Test", or Design For Test (DFT) at the chip, board or set of CCU's within a (sub)system. To truly perform "Design For Testability" at the fielded product or "Systems Level", "DFT" will require a much more advanced, agile and dynamic structure than what is typically characterized in common implementations. As a result, there is still a pseudo "duality of schools" on the understanding or interpretation of the role(s) of DFT, which depends upon the background and primary objectives of the project, program and leadership at the time of the discussion. Some of us must be ready to be comfortable in both schools at any time.

Ambiguity of the Terms, "DFT" and "System":

When the context of the use of the term, "DFT" begins to elevate to a target beyond a specific subsystem level, or to the "vehicle" or fielded "integrated systems" level, then here is where we often begin to witness confusion of the DFT term. At this juncture, we become introduced to the other common "failure" in the communication surrounding DFT as caused by the use of the term, "system level". So, in addition to "system level" being design domain limited, we begin to peel off another constraint. The DFT computation of its specific (sub)system totally separate and independent from its interaction with a myriad of comprehensive operating modes of and within any other integrated (sub)systems from a variety of suppliers and any surprise hosting of variable DFT requirements allocated downward and outward, if any.

DFT vs. “Diagnosis”:

An often overlooked understanding of DFT is that it is fundamentally limited within the boundaries of the “Test” discipline. When “Test” is understood to be performed in the production environment, then DFT becomes confined to looking strictly for “pass” or “failed” “test results”. Where’s the “Diagnostic CONCLUSIONS”? Where’s the ISOLATION?

Well, Fault Isolation can be described as a separate or companion “diagnostic reasoning” endeavor, sometimes referred to as “FI” (Fault Isolation) or “Diagnosis”. When “Fault Detection” is used with “Fault Isolation”, we may notice the combining of these activities as “FD/FI” or sometimes, simply, “FDI”.

Video: ATML-Based Integration of Diagnostics and Test Throughout the System Sustainment Life Cycle.

Calculating Fault Detection is SIMPLE – Calculating Fault Isolation is NOT Simple:

The Beautiful “Digital” Island of DFT is typically unable to equally effectively consider:

- The impact of mechanical, hydraulic, etc. or any other non-digital design domain (or mixtures thereof) of in both Fault Detection (FD) AND Fault Isolation (FI):
- Any “system level” FD/FI assessments as inclusive with, or as integrated within any complex system to include an evolving variety of design hierarchy and/or companion integrated subsystems provided by separate suppliers or external design activities or organizations.
- To interact beyond the boundaries of a simple assessment product paradigm and be “consumed” directly into the evolving operational or run-time diagnostic implementation technologies or maintenance philosophy/ies.

FD/FI Assessment Calculations – “Assigned TO Design” verses “Output FROM Design”:

If DFT is to quantify “testability”, but it is not directly transferable to the diagnostic implementation paradigm, then any resulting data produced within the assessment product must be “assigned to” a unique interpretation of the FD/FI integrity of that specific design piece.

Fault Isolation, or “Diagnosability”, calculations have been part & parcel to the traditional interpretation of the requirements of “Designing for Testability” at the “Fielded Product” (or, ‘Integrated Systems’) level. But the calculation of the “fielded product” level testability is not adequately performed by independently assessing the diagnostic integrity of any design piece without performing the assessment in the context of the fully fielded, integrated system(s) and including any number of variant design pieces in an operational paradigm.

Many design pieces and contributing design suppliers will have independent methods to calculate their independent and specific FD/FI, if required. To “roll-up” such assessment product data results that were “assigned to” these design pieces, assumes that a system level assessment shall include a thorough interpretation of the specific FD/FI analyses and any related stipulations reflected in each independent assessment product by that specific engineer and supplier.
There’s dozens of other designer-independent assumptions that must be absorbed when attempting to “incorporate” or “meld” FD/FI assessments (particularly when its required to extend such calculations with reliability, or failure rate data) when projecting fault group assumed constituencies at the next higher level(s) of the design(s).

Are Your FD/FI Assessment Products "Portable" to the Operational Paradigm?

Typically, any data provided by these traditional FD/FI (or any integrated systems' design discipline's) assessment approaches and products, unfortunately, is mostly relevant only at the time of design acceptance or at design delivery.

Such assessment products begin to diverge and become less relevant (including similarly-approached reliability & maintenance engineering assessment products) as the fielded system is maintained. In addition to many other asymmetrical operational stress factors realized within any integrated system, each occurrence of maintenance activity will forever change the failure characteristics of the fielded system(s). None of this dose of reality is able to be immediately or effectively reflective in common third-party or traditional, diagnostics-excluded, assessment products – regardless of design discipline inferred.

Fault Group constituencies (assigned to BIT codes or to any Health Management, ATE, IETM or any other diagnostic paradigm) will vary upon prior maintenance activities (Corrective Maintenance or Predictive Maintenance) due to the new failure properties of each component replaced – either as a result of its failure, its "assumed failure" or its "assumed impending failure". The investment into the building of eight or ten-digit decimal precision into the reliability-assigned failure rates becomes significantly less realized when not able to fully consider the volatility of fault group constituencies as a product of inferior diagnostic acumen. Disproportionately investing into Reliability Engineering (or PHM) at the expense of "in kind" of such prioritization/investment into Diagnostics Engineering exacerbates the size of the gaps between the failure rate data delivered in the assessment products and the replacement or suspected failure data realized in the sustainment of the fielded system(s). Predictive or Corrective maintenance become increasing out-of-script and expansive as this gap widens throughout the sustainment life cycle.

Alternatively, Advanced Diagnostic Engineering – meaning, not reduced to a constrained play at DFT or FD/FI, but rather a genuine and comprehensive interdisciplinary approach that “inadvertently” and seamlessly considers FD/FI (diagnostic engineering) as an integral component of the design development AND design sustainment life-cycle(s).

Test Coverage – verses Test Coverage Interference:

Calculating Test Coverage at the lower level pieces (chip, CCU, etc.) of the design are simplified in the fact that the FD/FI assessment products for that independent design piece is not considering its role or impact on the DFT at the highest levels of the fielded design. Traditional DFT methodologies lack richness in the seamless consideration of functional and/or failure effect flow up AND horizontally across (independently or externally-designed) integrated design subsystems when calculating the diagnostic integrity of the fielded system(s). It is critical to consider that additional integrated (sub)systems will have an undetermined impact on the “Test Coverage” at higher levels of design. The design engineer for the lower design piece simply brackets out that diagnostic concern. Hence, the “Test Coverage Interference” is not objectively considered. Additionally, the Test Coverage and the Test Coverage Interference MUST also consider the variable diagnostic capability when operating in a multitude of operational modes which will further reduce the FD/FI capability and consistency in the sustainment. Thus, corrective remediation or maintenance actions may not be conclusively applied, and if recorded for future repeated actions, may lead to undetermined sustainment costs in NFFs, CND’s and False System Aborts.

More background on the impact of “Test Coverage” in Test, Diagnostic, Reliability and Safety Assessment Products can be found here: “Using the Fault Tree Analysis as a Diagnostic Tool”
https://www.linkedin.com/pulse/using-fault-tree-analysis-diagnostic-tool-craig-de-paul?trk=prof-post

Assessment Products for DFT should be a Direct Output from the (evolving) Design:

When the Design is captured in ***eXpress***, the entire diagnostic integrity is captured and can be FULLY VALIDATED at every level, with any subsystem(s), with any design piece, and mixture of design domains, and with any updated design pieces considered or integrated into the fully fielded design. The variance and limitations of the Test Coverage are simple and immediate outputs from the ***eXpress*** model. The BIT error codes can be fully validated for any mode and the customer can choose any number of faults he may desire to perform in any maintenance demo. A video on “desktop” DIAGNOSTIC VALIDATION will be posted for a general audience in a few weeks – but a brief look at page 4 of this document will provide a small hint: ***eXpress*** Newsletter, Fall 2015 (http://www.dsiintl.com/Resources/Newsletters/Fall%202015.pdf).

The FD/FI assessment produced at any level is actually fully transferable to the field AND to any Run-Time implementation or evolving paradigm.

All assessment products produced from ***eXpress*** are OUTPUTS from the fully-integrated and captured design and available at any time during the design development AND the (evolving) sustainment paradigm.

Since, DSI has had a dog in the fight long ago, it has continued to foster and broaden the reach of DFT ever since. Not everyone has been aware of, not just DSI’s pioneering of “Designing for Testability”, but its continued innovation in the integrated (re)use of any investment(s) into this design discipline as well as any companion design AND support discipline (RAMS).

Other Related videos:

ATML-Based Integration of Diagnostics and Test

Establishing an FHA Architecture

Diagnostically-informed FMECA & FTA:

Generating a "Turn-Key" (Diagnostics-Informed) FMECA:

Topic Notes
Craig DePaul
President – CEO
DSI International, Inc.

DSI International, Inc. is a leading provider
of
World Class diagnostic engineering tools and services.

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