Strathclyde Engagement with the National HVDC Centre: Development and Validation of LCC HVDC System Impedance Models

Doc. Type:	Technical report	*Date:*	**19/03/2021**
Doc. Nº:	**USTRATH-HVDC Centre-P2-001**	*Issue:* ***1***	*Page:* **1** *of* **37**
Title:	Development and Validation of LCC HVDC System Impedance Models		

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Executive summary

Previous studies carried out as part of the joint Strathclyde-The National HVDC Centre collaborative work have developed frequency domain network / MMC converter models adequate for small signal stability analysis. Recommendations for specification and operation requirement of MMC based HVDC systems have been proposed when obtaining frequency domain HVDC converter models. Using the developed network and MMC small-signal impedance models, the stability of multiple converter systems has been studied. This study approach uses small signal methods to identify with good alignment to EMT dynamic simulation those operating states of MMC based HVDC systems and the transmission networks between them where interactions between converters most likely may arise. In a transmission network however MMC converters are not the only dominant source of frequency dependency and both the effect of LCC HVDC converters or the cumulative effect of similar Wind Turbine generators frequency dependency also has a bearing on what operational conditions may give rise to interaction, between what devices and should then be considered further within EMT analysis.

This report extends the previous modelling work and concentrates on the development of small-signal LCC converter and LCC HVDC system models. The development of the analytical impedance model intends to provide further insight into the impact of circuit and control structure/parameters on system impedance, and similarly highlight the considerations that need to be considered when an LCC HVDC connection is defining its frequency-dependent impedance accurately ahead of a network scale small-signal interaction study being performed. The developed impedance models can then be used for assessing stability and interactions between different converters (e.g., MMC, LCC, wind farm, etc.).

The behaviour of a LCC is non-linear in nature given thyristor switching, and hence the small signal model needs to be derived from the given operating mode of the thyristors linearised from time domain operation of the given model. An analytical model similar to that of the MMC describing a 2x2 admittance matrix at the AC terminals can then be obtained to describe the small signal behaviour of the LCC system. This analytical model is validated using measurements from the time domain simulation model.

The obtained LCC impedance/admittance results show that:

- The admittance matrix of an LCC system can be represented by a 2x2 matrix, similar to other converter systems. Thus, a network that contains different converter technologies can be assessed by considering the impedance of each converter and the AC network.
- LCC converter operating point such as power and firing angle affects the impedance, though less significantly than has been observed in VSCs, e.g., MMC.
- The control mode (e.g., DC current control, DC voltage control) impacts the converter admittance. However, the controller parameters (e.g., PLL and controller gains etc.) only have a small impact on the converter admittance.

- AC filters significantly affect the overall impedance especially at a higher frequency range, e.g., above 100 Hz. As such which tuned filters are in service for a given operating point and operating mode of the converter must be specified and included in the reduction undertaken.
- For an LCC transmission system, the AC impedance at one terminal is affected by the DC side impedance of the other terminal, while DC side impedance is affected by the converter control mode and the AC network condition (network strength) for which the converter is connected to.
- Thus, LCC AC impedance at one terminal can be affected by the AC network condition of the other terminal, though such impact is mainly on the low-frequency area, e.g., below 100 Hz. This mainly impact on the AC impedance of the rectifier side during low network strength at the inverter terminal.
- As such a range of short circuit strengths to define the AC network condition of the external network at different times of study of the GB system for interactions below 100Hz is advisable, especially cases with the lowest possible SCR at the inverter terminal should be considered when studying the stability of the rectifier AC system.

1 General introduction

To assess the stability of power networks with large numbers of converters, it has been shown that the impedance-based approach is advantageous and effective, as it avoids the need to remodel each converter and repeat its loop stability analysis when the grid changes, or when more converters are connected to the same grid.

Building on the previous work on the development of frequency-domain network and MMC converter models, further development work on the LCC converter and LCC HVDC system models are carried out such that the stability and interactions between different converter technologies can be studied.

Due to thyristor commutation, the operation of each phase in an LCC converter contains different stages and thus the AC phase current is a piecewise function of time. In the modelling method adopted here, Fourier series are used to mathematically represent the system model as a multiple periodical system which is then linearized and converted to the frequency domain to obtain the converter small-signal impedance. To validate the developed analytical models, frequency sweep measurements using time-domain simulation models are carried out.

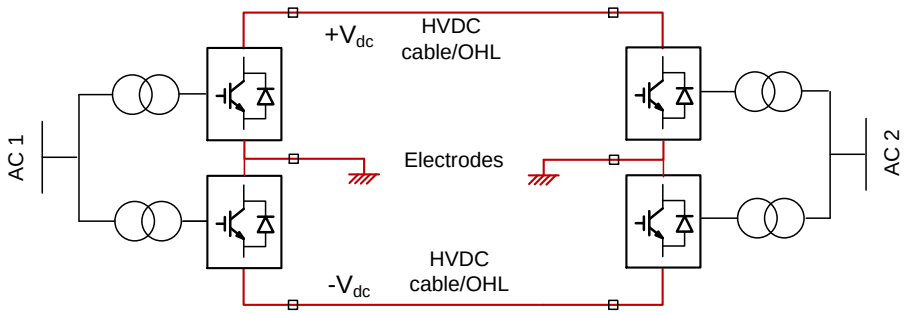
The impact of LCC converter operating point including active power and firing angle, control mode and control parameters on converter AC impedance is investigated. The overall AC impedances including the converter and AC filters are obtained. The DC impedance of the LCC converter is also calculated which is then used to obtain the AC impedance of the other terminal. Finally, the impact of AC network condition on the impedance of the other converter terminal is investigated.

2 Steady-state model of LCC converter

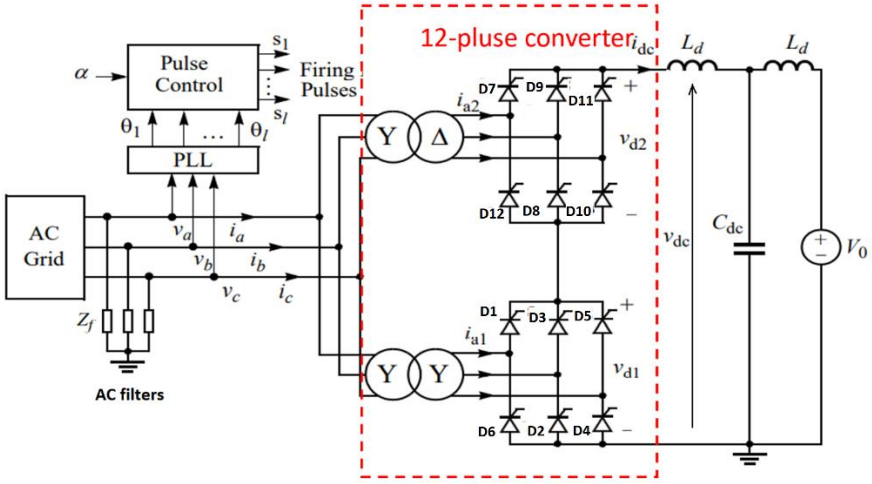
In this section, considering the operation nature of an LCC converter as a nonlinear time-varying system, its operation and waveforms are represented using piecewise functions of time. Fourier series and harmonic state space (HSS) modelling approach are then used to represent the system model as a multiple periodical system.

2.1 General system configuration and operation

Figure 1(a) shows the typical layout of a two-terminal bipole LCC HVDC scheme, in which each converter terminal contains a positive pole and a negative pole. As an example, Figure 1(b) shows the configuration of the positive pole on the rectifier station. As seen, a typical converter pole contains a 12-pulse LCC converter and switched AC filters which usually contain high pass filters and tuned filters around the 12^{th} and 24^{th} harmonics.



(a) Typical bipole LCC HVDC layout



(b) One LCC pole

Figure 1 Typical LCC HVDC system

By controlling the firing angles of the thyristors synchronized to the network voltage (via the phase-locked loop – PLL as shown in Figure 1(b)), the generated DC voltage can be controlled. Due to the existence of the AC side reactance, the switching of the thyristors (commonly called commutation) is not instantaneous, requiring a finite time (the commutation period). Taking one 6-pulse bridge (e.g., the bottom rectifier bridge in Figure 1 (b)) as an example, Figure 2 shows the typical waveforms during the commutation from D5 (phase *c*) to D1 (phase *a*). As can be seen from Figure 2(a), when D1 is turned on after a delay angle of α, both D5 and D1 conduct for a period of μ (commutation period). During the commutation period, the two phases on the AC side are joined together at the DC side terminal, each carrying a varying portion of the DC side current, i.e. the currents in these two phases are varying with time, but they should always sum to the DC side current. At the end of the commutation period, the current in the phase that is commutating to a non-conduction state (phase c in Figure 2) is approaching zero while the current in the phase that is commutating to a direct conduction state (phase a in Figure 2) is approaching the DC current.

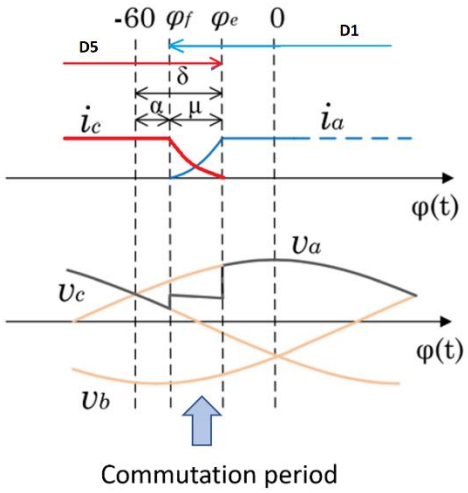


Figure 2 Typical waveforms during thyristor commutation

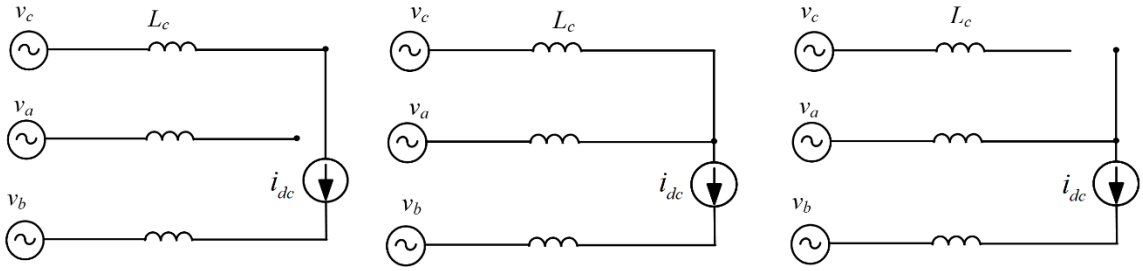


Figure 3 Equivalent circuits during LCC commutation (D5 to D1)

Figures 3 (a)-(c) show the equivalent circuits before, during and after commutation. These time intervals associated with the three stages are commonly referred to as the direct conduction period, the commutation period, and the non-conduction period. The current for each phase during the three different periods can be derived considering the relevant equivalent circuits. Thus, the AC current waveform of each phase is a piecewise function of time and can be considered as the sum of three periodic sub-functions each describing a distinct portion of the AC current waveform during a certain interval of time.

Figure 4 shows the outline of the modelling procedure that will be used to develop a small signal LCC converter system model. The time-varying system model will be developed and due to the fact that both the voltage and current are time-varying and piecewise functions, Fourier expansion is then used to mathematically represent the system model as a multiple periodical system using HSS method, at a particular operating point. The system will be linearized in the time domain and then converted to a time-invariant system in the frequency domain.

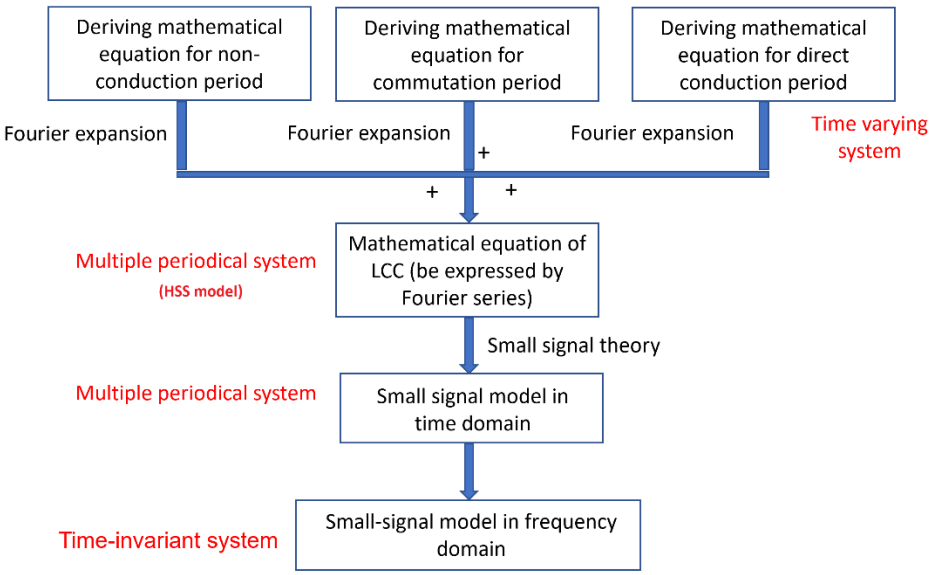


Figure 4 Outline of small-signal LCC modelling procedure

2.2 Commutation inductor voltage expression

Figure 5 shows the detailed circuit of LCC commutation from conduction mode D1-D2 to D3-D2 (phases *a* and *c* to phases *b* and *c*). According to Figure 5, the relationship between AC side and DC side can be expressed as:

$$L_c \frac{di_a}{dt} = v_a - V_+, \quad L_c \frac{di_b}{dt} = v_b - V_+, \quad L_c \frac{di_c}{dt} = v_c + V_- \tag{1}$$

$$2L_c \frac{di_a}{dt} - L_c \frac{di_{dc}}{dt} = v_a - v_b \tag{2}$$

where L_c is the commutation inductor on the AC side.

Considering the impact of phase 'a' current by the DC current and AC voltages separately, i_a can be represented as two parts as:

$$2L_c \frac{di_{1a}}{dt} = L_c \frac{di_{dc}}{dt} \tag{3}$$

$$L_c \frac{di_{2a}}{dt} = v_{coma} = 0.5v_a - 0.5v_b \tag{4}$$

where v_{coma} is the voltage across the commutation inductor L_c for phase a.

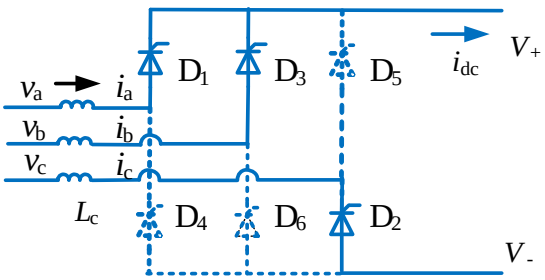


Figure 5 LCC commutation circuit

In one fundamental cycle, the commutation process occurs six times (one for each thyristor). As each is connected to two thyristors and each thyristor is switched on and off once per fundamental period, four commutations occur in each phase. According to (4), the voltage across the commutation inductance in phase *a* can be expressed as:

$$v_{coma} = S_{coma-a}v_a + S_{coma-b}v_b + S_{comc-c}v_c \tag{5}$$

where $S_{coma-a,b,c}$ are the switching functions defining the relationships between the AC voltage of the phase *a* inductor and the three-phase source voltages. According to (5) and (4), $S_{coma-a,b,c}$ equals to 0.5 or -0.5 during the commutation period, and to 0 during the non-conduction and direct conduction periods. Thus the waveforms of the switching functions $S_{coma-a,b,c}$ are be derived as shown in Figure 6.

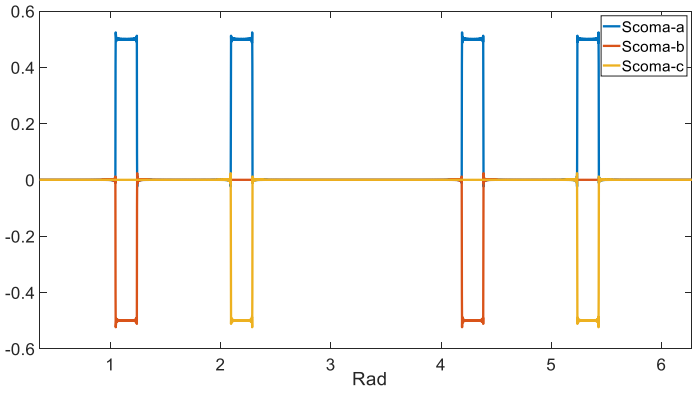


Figure 6 the wave of switching function $S_{coma-a,b,c}$

The switching functions can be written by Fourier expressions as

$$\begin{aligned}
S_{coma-a} &= \frac{\mu_0}{\pi} + \sum_{m=-\infty}^{+\infty}\left[\frac{1}{2\pi m}\sin\left(\frac{m\mu_0}{2}\right)\left(e^{-j\pi m/3} + e^{-j2\pi m/3} + e^{-j4\pi m/3} + e^{-j5\pi m/3}\right)e^{-jm(-\omega_0 t + 0.5\mu_0 + \alpha_0)}\right] \\
S_{coma-b} &= -\frac{\mu_0}{2\pi} - \sum_{m=-\infty}^{+\infty}\left[\frac{1}{2\pi m}\sin\left(\frac{m\mu_0}{2}\right)\left(e^{-j\pi m/3} + e^{-j4\pi m/3}\right)e^{-jm(-\omega_0 t + 0.5\mu_0 + \alpha_0)}\right] \\
S_{coma-c} &= -\frac{\mu_0}{2\pi} - \sum_{m=-\infty}^{+\infty}\left[\frac{1}{2\pi m}\sin\left(\frac{m\mu_0}{2}\right)\left(e^{-j2\pi m/3} + e^{-j5\pi m/3}\right)e^{-jm(-\omega_0 t + 0.5\mu_0 + \alpha_0)}\right]
\end{aligned} \tag{6}$$

where μ_0 is the commutation overlap angle, α_0 is the firing angle, ω_0 is the fundamental frequency, and m is the harmonic order.

Figure 7 compares the simulated inductor voltage v_{coma} with calculated waveform using (5) and (6) when harmonic orders of 100 are considered. As can be seen, the voltages match well which validate its analytical expressions.

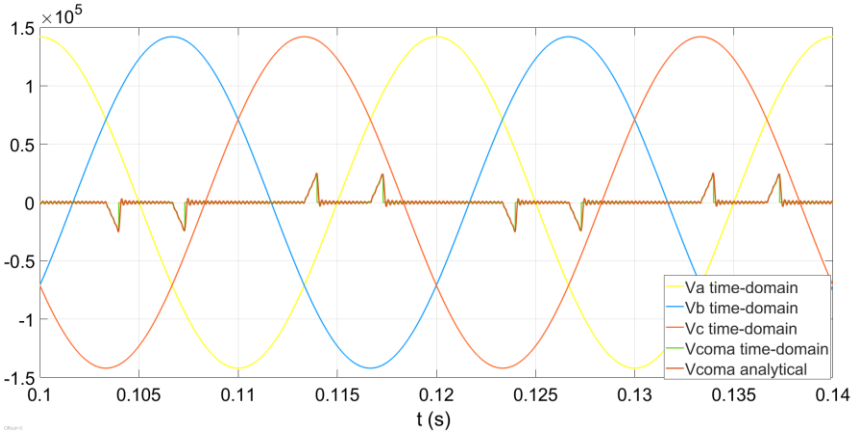


Figure 7 Comparison of simulated and calculated AC inductor voltages

2.3 DC voltage expression using AC side voltage

Similar to the AC inductor voltage v_{coma}, the DC voltage v_{dc} can also be expressed as a combination of the three-phase AC voltage as:

$$v_{dc} = S_{dc-a}v_a + S_{dc-b}v_b + S_{dc-c}v_c \tag{7}$$

where $S_{dc-a,b,c}$ are the switching functions from three-phase voltage to DC voltage.

As shown in Figure 5, during commutation from D1 to D3, for the direct conduction period, v_a is applied to the DC side while v_c is reversely applied to the DC side, so S_{dc-a}=1 and S_{dc-c}=-1. During the commutation period, v_a and v_b are both applied to the DC side, and thus S_{dc-a}=0.5 and S_{dc-b}=0.5 while v_c is still reversely applied to DC side, so S_{dc-c}=-1. For the non-conduction period, only D2 and D3 are on so S_{dc-a}=0, S_{dc-b}=1, and S_{dc-c}=-1. The overall waveforms of $S_{dc-a,b,c}$ across one fundamental period are shown in Figure 8, with the highlighted period referring to the scenario described earlier.

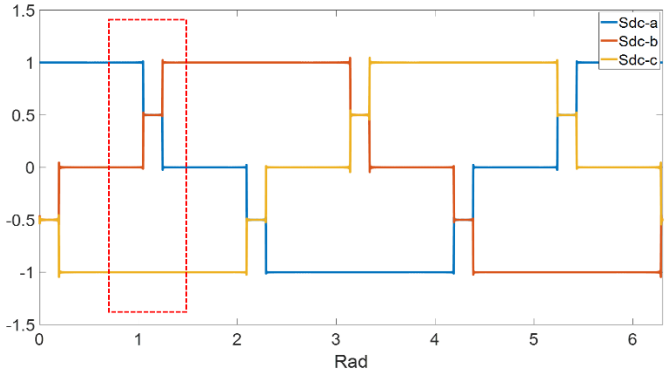


Figure 8 DC voltage switch function

The switching functions of $S_{dc\text{-}a,b,c}$ in Fourier form can be expressed as:

$$S_{dc-a} = \sum_{m=-\infty}^{+\infty} \left\{ \frac{1}{\pi m}\left[\sin\left(\frac{m\pi}{3}\right)+\sin\left(\frac{2m\pi}{3}\right)\right] e^{-jm(-\omega_0 t+\alpha_0)} - \frac{1}{\pi m}\sin\left(\frac{m\mu_0}{2}\right)\left[\sin\left(\frac{m\pi}{3}\right)+\sin\left(\frac{2m\pi}{3}\right)\right] e^{-jm(-\omega_0 t+\alpha_0+0.5\mu_0)+j0.5\pi} \right\}$$

$$S_{dc-b} = \sum_{m=-\infty}^{+\infty} \left\{ \frac{1}{\pi m}\left[\sin\left(\frac{m\pi}{3}\right)+\sin\left(\frac{2m\pi}{3}\right)\right] e^{-jm(-\omega_0 t+\alpha_0+2\pi/3)} - \frac{1}{\pi m}\sin\left(\frac{m\mu_0}{2}\right)\left[\sin\left(\frac{m\pi}{3}\right)+\sin\left(\frac{2m\pi}{3}\right)\right] e^{-jm(-\omega_0 t+\alpha_0+0.5\mu_0+2\pi/3)+j0.5\pi} \right\}$$

$$S_{dc-c} = \sum_{m=-\infty}^{+\infty} \left\{ \frac{1}{\pi m}\left[\sin\left(\frac{m\pi}{3}\right)+\sin\left(\frac{2m\pi}{3}\right)\right] e^{-jm(-\omega_0 t+\alpha_0-2\pi/3)} - \frac{1}{\pi m}\sin\left(\frac{m\mu_0}{2}\right)\left[\sin\left(\frac{m\pi}{3}\right)+\sin\left(\frac{2m\pi}{3}\right)\right] e^{-jm(-\omega_0 t+\alpha_0+0.5\mu_0-2\pi/3)+j0.5\pi} \right\} \quad (8)$$

Figure 9 compares the measured DC voltage in time domain simulation with calculated waveforms using (7) and (8) when harmonic orders of 100 are considered. As can be seen, the DC voltages match well which validate its analytical expressions.

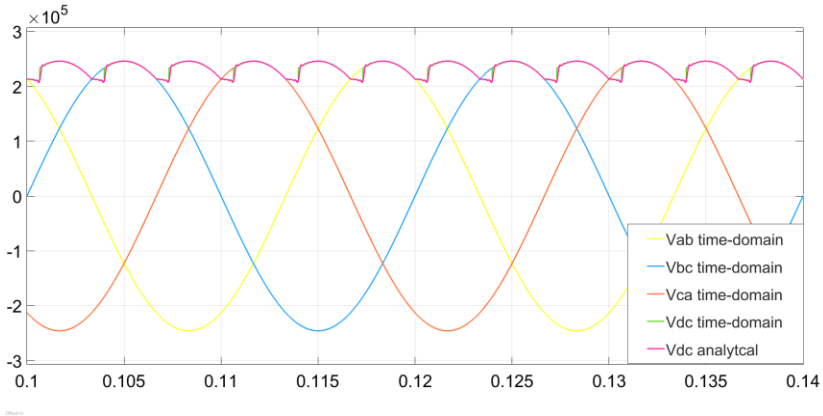


Figure 9 DC voltage validation

2.4 DC current to DC voltage

As shown in Figures 3(a) and (c), during the direct and non-conduction periods, two AC side phases are connected in series to the DC side. During the commutation period, the two commutating AC phases are connected in parallel to the DC side terminal which is then in series with the third conducting phase as illustrated in Figure 3(b). The voltage on the DC side due to these two circuit configurations can be expressed accordingly. For the direct and non-conduction periods:

$$v_{dc} = -2L_c \frac{di_{dc}}{dt} - 2Ri_{dc} \tag{9}$$

where R is the equivalent resistance of the AC commutation inductance.

For the commutation period:

$$v_{dc} = -\frac{3}{2} L_c \frac{di_{dc}}{dt} - \frac{3}{2} Ri_{dc} \tag{10}$$

Combining (9) and (10), the DC voltage in one fundamental cycle can be described using a switching function $S_{vdc\text{-}idc}$ as:

$$v_{dc} = S_{vdc-idc}\left(L_c \frac{di_{dc}}{dt} - Ri_{dc} \right) \tag{11}$$

The waveforms of $S_{vdc\text{-}idc}$ are shown in Figure 10 and the Fourier expansion is given as:

$$\begin{aligned} S_{vdc-idc} &= 1.5\mu_0 - 2 \\ &- \frac{1}{4\pi m} \begin{bmatrix} e^{-jm(-\omega_0 t + pi/3 + \alpha_0 + \mu_0)} - e^{-jm(-\omega_0 t + pi/3 + \alpha_0)} + e^{-jm(-\omega_0 t + 2pi/3 + \alpha_0 + \mu_0)} - e^{-jm(-\omega_0 t + 2pi/3 + \alpha_0)} \\ + e^{-jm(-\omega_0 t + pi + \alpha_0 + \mu_0)} - e^{-jm(-\omega_0 t + pi + \alpha_0)} + e^{-jm(-\omega_0 t + 4pi/3 + \alpha_0 + \mu_0)} - e^{-jm(-\omega_0 t + 4pi/3 + \alpha_0)} \\ e^{-jm(-\omega_0 t + 5pi/3 + \alpha_0 + \mu_0)} - e^{-jm(-\omega_0 t + 5pi/3 + \alpha_0)} + e^{-jm(-\omega_0 t + \alpha_0 + \mu_0)} - e^{-jm(-\omega_0 t + \alpha_0)} \end{bmatrix} \end{aligned} \tag{12}$$

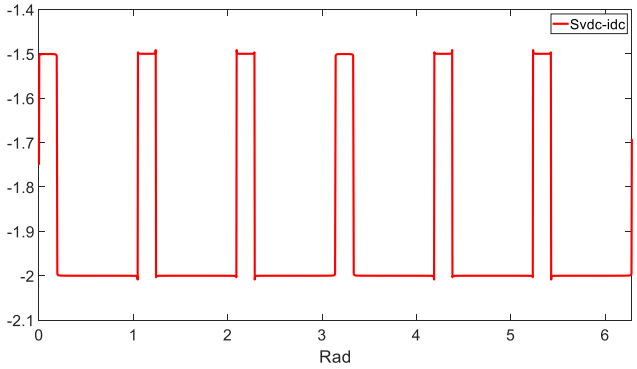


Figure 10 DC current to DC voltage switching function

2.5 DC circuit dynamic

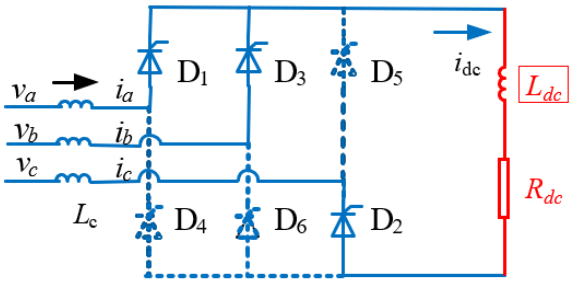


Figure 11 Connected DC circuit

The analysis associated with the DC side has assumed to be an ideal current source. To include DC side dynamics, the DC side terminals are connected to a DC side circuit represented by a resistor R_{dc} and inductor L_{dc} in series as shown in Figure 10. The state dynamic equation for the DC side $R_{dc}L_{dc}$ circuit is written:

$$L_{dc}\frac{di_{dc}}{dt} = -R_{dc}i_{dc} + v_{dc} \tag{13}$$

2.6 DC current to AC current

As shown in (3), part of the phase *a* current, i.e., i_{1a}, is affected by the DC current so it is necessary to derive the relationship between such AC current component and the DC current, also considering the different conduction states.

- For the non-conduction period, DC current does not flow through the AC phase, so the gain between the AC current and DC current can be considered as 0.
- For the direct conduction period the DC circuit is directly connected with the AC phase, so the gain is 1.
- During the commutation period, the DC current can be considered as splitting across two AC phases, so the gain becomes 0.5.

Thus, in one fundamental cycle the relationship between the voltage across the commutation inductor and DC current is illustrated as:

$$\begin{aligned} L_c\frac{di_{1a}}{dt} &= S_{coma-idc}L_c\frac{di_{dc}}{dt} \\ L_c\frac{di_{1b}}{dt} &= S_{comb-idc}L_c\frac{di_{dc}}{dt} \\ L_c\frac{di_{1c}}{dt} &= S_{comc-idc}L_c\frac{di_{dc}}{dt} \end{aligned} \tag{14}$$

where the three-phase waveforms of $S_{coma,b,c\text{-}idc}$ are shown in Figure 12.

Similarly, the switching functions of $S_{coma,b,c\text{-}idc}$ in Fourier form can be expressed as:

$$S_{coma-idc} = \sum_{m=-\infty}^{+\infty} \left\{ \left[\frac{1}{\pi m} \sin\left(\frac{m\pi}{3}\right) + \sin\left(\frac{2m\pi}{3}\right) \right] e^{-jm(-\omega_0 t+\alpha_0)} - \frac{1}{\pi m} \sin\left(\frac{m\mu_0}{2}\right) \left[\sin\left(\frac{m\pi}{3}\right) + \sin\left(\frac{2m\pi}{3}\right) \right] e^{-jm(-\omega_0 t+\alpha_0+0.5\mu_0)+j0.5\pi} \right\}$$

$$S_{comb-idc} = \sum_{m=-\infty}^{+\infty} \left\{ \left[\frac{1}{\pi m} \sin\left(\frac{m\pi}{3}\right) + \sin\left(\frac{2m\pi}{3}\right) \right] e^{-jm(-\omega_0 t+\alpha_0+2\pi/3)} - \frac{1}{\pi m} \sin\left(\frac{m\mu_0}{2}\right) \left[\sin\left(\frac{m\pi}{3}\right) + \sin\left(\frac{2m\pi}{3}\right) \right] e^{-jm(-\omega_0 t+\alpha_0+0.5\mu_0+2\pi/3)+j0.5\pi} \right\}$$

$$S_{comc-c} = \sum_{m=-\infty}^{+\infty} \left\{ \left[\frac{1}{\pi m} \sin\left(\frac{m\pi}{3}\right) + \sin\left(\frac{2m\pi}{3}\right) \right] e^{-jm(-\omega_0 t+\alpha_0-2\pi/3)} - \frac{1}{\pi m} \sin\left(\frac{m\mu_0}{2}\right) \left[\sin\left(\frac{m\pi}{3}\right) + \sin\left(\frac{2m\pi}{3}\right) \right] e^{-jm(-\omega_0 t+\alpha_0+0.5\mu_0-2\pi/3)+j0.5\pi} \right\} \quad (15)$$

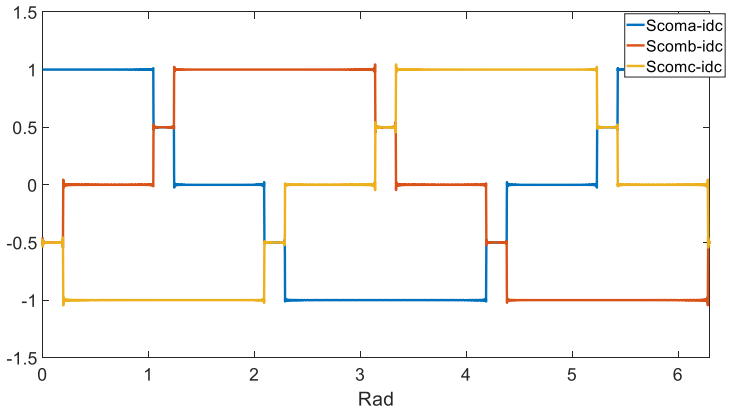


Figure 12 The switching function $S_{coma,b,c\text{-}idc}$

2.7 HSS model for LCC system

The analytical models of the system previously derived can be combined together to form a complete system model based on HSS principle as shown in Figure 13. The input is the three-phase AC voltage v_{abc} and the output is the three-phase current i_{abc}. To validate the derived mathematical HSS model, the calculated AC current and DC voltage waveforms are compared to those obtained from the time domain model, as shown in Figure 14. As can be seen, the calculated results using the HSS model match well with those obtained from simulation, indicating the correctness and accuracy of the HSS model.

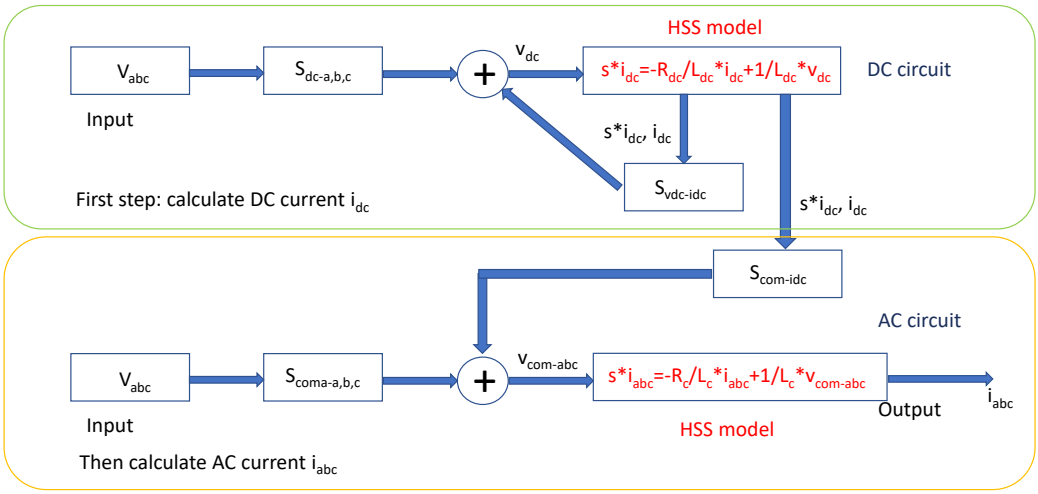
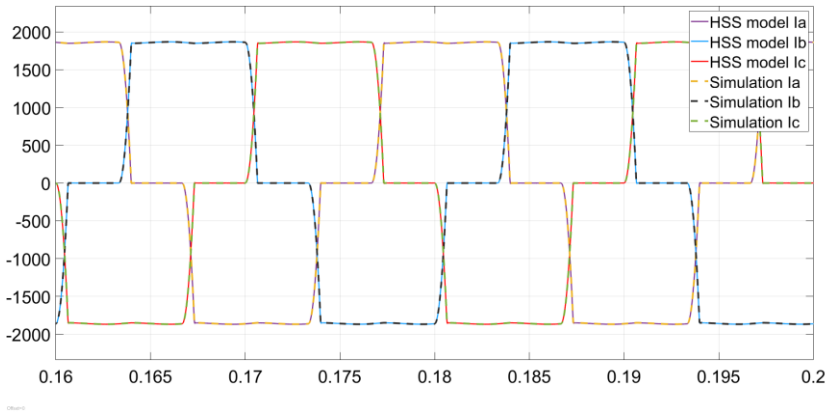
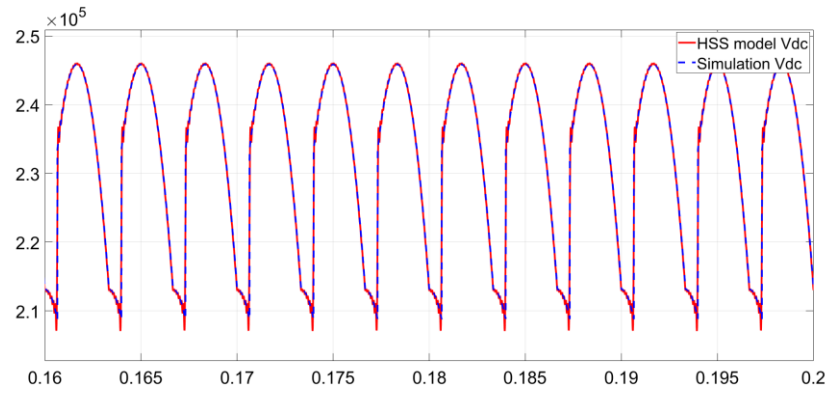


Figure 13 Mathematical model structure



(a) Three-phase i_{abc}



(b) DC voltage v_{dc}

Figure 14 Comparison between the HSS model calculation and time-domain simulation results

3 Small-signal LCC converter model

To accurately represent the time-variant piecewise AC current and DC voltage waveforms, HSS models are required as shown in Section 2.7. However, since the dominant 11th and 13th harmonics do not directly affect the small-signal impedance created by the fundamental components, the development of the small-signal model can be simplified without affecting the accuracy of the impedance results by only considering the fundamental components, as will be validated in Section 4.

3.1 DC side voltage dynamic

As shown in Figure 13, the DC side voltage is determined by the AC voltage and DC current, which can be expressed as:

$$v_{dc} = S_{dc-a}v_a + S_{dc-b}v_b + S_{dc-c}v_c + S_{vdc-idc}\left(L_c\frac{di_{dc}}{dt} + Ri_{dc}\right) \tag{16}$$

In (8) the harmonic order of the switching function $S_{dc\text{-}a,b,c}$ m is equal to 1 and -1, while in (12), the harmonic order of the switching function $S_{vdc\text{-}idc}$ m is 0 (as high order harmonics are neglected). Substituting the switching function into (16) yields:

$$\begin{aligned} v_{dc} = {} & \frac{\sqrt{3}}{\pi}\left[\cos(\omega_0 t-\alpha_0)+\cos(\omega_0 t-\mu_0-\alpha_0)\right]v_a + \frac{\sqrt{3}}{\pi}\left[\cos\left(\omega_0 t-\alpha_0-\frac{2\pi}{3}\right)+\cos\left(\omega_0 t-\mu_0-\alpha_0-\frac{2\pi}{3}\right)\right]v_b \\ & + \frac{\sqrt{3}}{\pi}\left[\cos\left(\omega_0 t-\alpha_0+\frac{2\pi}{3}\right)+\cos\left(\omega_0 t-\mu_0-\alpha_0+\frac{2\pi}{3}\right)\right]v_c + (1.5\mu_0-2)\left(L_c\frac{di_{dc}}{dt}+Ri_{dc}\right) \end{aligned} \tag{17}$$

The voltage v_a, v_b and v_c can be described in the positive-negative sequence pn frame as:

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 1 & 1 & 1 \\ e^{j4\pi/3} & e^{j2\pi/3} & 1 \\ e^{j2\pi/3} & e^{j4\pi/3} & 1 \end{bmatrix}\begin{bmatrix} v_p \\ v_n \\ v_0 \end{bmatrix} \tag{18}$$

Combining (17) and (18), the relationship between the DC voltage and the AC voltage in pn frame is described as:

$$v_{dc} = \frac{\sqrt{3}}{2\pi}\left\{\begin{aligned} & \left[\cos(\omega_0 t-\alpha)-j\sin(\omega_0 t-\alpha)+\cos(\omega_0 t-\alpha-\mu)-j\sin(\omega_0 t-\alpha-\mu)\right]v_p \\ & +\left[\cos(\omega_0 t-\alpha)+j\sin(\omega_0 t-\alpha)+\cos(\omega_0 t-\alpha-\mu)+j\sin(\omega_0 t-\alpha-\mu)\right]v_n \end{aligned}\right\} + (1.5\mu_0-2)\left(L_c\frac{di_{dc}}{dt}+Ri_{dc}\right) \tag{19}$$

Linearizing (19) and transferring into the frequency domain, the DC voltage deviation is derived as:

$$\begin{aligned} \Delta v_{dc} = {} & \frac{\sqrt{3}}{2\pi}\left[\left(e^{j\alpha_0}+e^{j\delta_0}\right)\Delta v_p + \left(e^{-j\alpha_0}+e^{-j\delta_0}\right)\Delta v_n + \left(je^{j\alpha_0}V_p - je^{-j\alpha_0}V_n\right)\Delta\alpha + \left(je^{j\delta_0}V_p - je^{-j\delta_0}V_n\right)\Delta\delta\right] \\ & + L_c(1.5\mu_0-2)(s-j\omega_0)\Delta i_{dc} \end{aligned} \tag{20}$$

where $\delta_0=\alpha_0+\mu_0$. α_0, μ_0, V_p and V_n represent the steady-state values, while Δ denotes small-signal variables.

According to (20) the deviations $\frac{\Delta v_{dc}}{\Delta v_p}$, $\frac{\Delta v_{dc}}{\Delta v_n}$, $\frac{\Delta v_{dc}}{\Delta i_{dc}}$, $\frac{\Delta v_{dc}}{\Delta \alpha}$ can be derived.

3.2 Commutation overlap angle and firing angle dynamics

As discussed in Section 1.1, the phase *b* current can be divided to two parts:

$$i_b=i_{1b}+i_{2b} \tag{21}$$

$$2L_c\frac{di_{1b}}{dt}=L_c\frac{di_{dc}}{dt} \tag{22}$$

$$L_c\frac{di_{2b}}{dt}=0.5v_b-0.5v_a \tag{23}$$

Defining times (phase angles) at the beginning and end of commutation are φ and φ_f, respectively, the difference between φ_f and φ is thus the overlap angle μ. When the phase *b* current is equal to the DC current, the commutation is completed as shown in Figure 2. Thus, the relationship between phase *b* current and DC current can be described as:

$$i_b\left(\varphi_f\right)=i_{dc}\left(\varphi_f\right) \tag{24}$$

Integrating (22) results in i_{1b} as:

$$i_{1b}\left(\varphi_f\right)=0.5\left[i_{dc}\left(\varphi_f\right)-i_{dc}(\varphi)\right] \tag{25}$$

where $i_{dc}(\varphi)$ represents the DC current at the beginning of the commutation.

At the end of the commutation, (21) is rewritten as:

$$i_b\left(\varphi_f\right)=i_{1b}\left(\varphi_f\right)+i_{2b}\left(\varphi_f\right) \tag{26}$$

Substituting (24) and (25) into (26) yields:

$$i_{2b}\left(\varphi_f\right)-0.5i_{dc}\left(\varphi_f\right)-0.5i_{dc}(\varphi)=0 \tag{27}$$

According to (18) the current i_{2b} is transferred into pn frame as:

$$i_{2b}\left(\varphi_f\right)=i_{2p}\left(\varphi_f\right)e^{j(4\pi/3+\varphi_f)}+i_{2n}\left(\varphi_f\right)e^{j(2\pi/3+\varphi_f)}-\left[i_{2p}(\varphi)e^{j(4\pi/3+\varphi)}+i_{2n}(\varphi)e^{j(2\pi/3+\varphi)}\right] \tag{28}$$

Substituting (28) into (27) and linearizing the equation yield:

$$\begin{aligned}&-0.5\Delta i_{dc}(\varphi)-0.5\Delta i_{dc}(\varphi_f)+\Delta i_{2p}(\varphi_f)e^{j(4\pi/3+\varphi_f)}+je^{j(4\pi/3+\varphi_f)}I_{2p}\Delta\delta+\Delta i_{2n}(\varphi_f)e^{j(2\pi/3+\varphi_f)}+je^{j(2\pi/3+\varphi_f)}I_{2n}\Delta\delta\\&-\left[\Delta i_{2p}(\varphi)e^{j(4\pi/3+\varphi)}+je^{j(4\pi/3+\varphi)}I_{2p}\Delta\alpha+\Delta i_{2n}(\varphi)e^{j(2\pi/3+\varphi)}+je^{j(2\pi/3+\varphi)}I_{2n}\Delta\alpha\right]=0\end{aligned}\tag{29}$$

The Laplace transform of a typical variable x at time φ_f can be expressed by multiplying $L[x(\varphi)]$ by the transportation lag $e^{-(s-j\omega_0)\mu/\omega_0}$ as:

$$L\left[x(\varphi)\right]=e^{-(s-j\omega_0)\mu/\omega_0}L\left[x\left(\varphi_f\right)\right]\tag{30}$$

Thus, the angle δ=μ+α deviation can be derived as:

$$\Delta\delta=\Delta\mu+e^{-(s-j\omega_0)\mu/\omega_0}\Delta\alpha\tag{31}$$

According to (30) and (31), (29) can be rewritten as:

$$\begin{aligned}&-\frac{1}{2}\Delta i_{dc}\left(1+e^{-(s-j\omega_0)\mu_0/\omega_0}\right)+\Delta i_{2p}\left(e^{j(4\pi/3+\delta_0)}-e^{-(s-j\omega_0)\mu_0/\omega_0}e^{j(4\pi/3+\alpha_0)}\right)+\Delta i_{2n}\left(e^{j(2\pi/3+\delta_0)}-e^{-(s-j\omega_0)\mu_0/\omega_0}e^{j(2\pi/3+\alpha_0)}\right)\\&+\Delta\alpha e^{-(s-j\omega_0)\mu_0/\omega_0}\left(I_{2p}je^{j(4\pi/3+\delta_0)}-I_{2p}je^{j(4\pi/3+\alpha_0)}+I_{2n}je^{j(2\pi/3+\delta_0)}-I_{2n}je^{j(2\pi/3+\alpha_0)}\right)+\\&\Delta\mu\left(I_{2p}je^{j(4\pi/3+\delta_0)}+I_{2n}je^{j(2\pi/3+\delta_0)}\right)=0\end{aligned}\tag{32}$$

where Δi_{2p} and Δi_{2n} are defined as:

$$\begin{bmatrix}\Delta i_{2p}\\ \Delta i_{2n}\end{bmatrix}=\begin{bmatrix}\frac{1}{sL_c} & 0\\ 0 & \frac{1}{sL_c}\end{bmatrix}\begin{bmatrix}\Delta v_p\\ \Delta v_n\end{bmatrix}\tag{33}$$

I_{2p} and I_{2n} are the steady state values obtained as:

$$\begin{bmatrix}\Delta I_{2p}\\ \Delta I_{2n}\end{bmatrix}=\begin{bmatrix}\frac{1}{j\omega_0 L_c} & 0\\ 0 & \frac{1}{j\omega_0 L_c}\end{bmatrix}\begin{bmatrix}V_p\\ V_n\end{bmatrix}\tag{34}$$

Combining (32) and (33), the deviations $\frac{\Delta\mu}{\Delta v_p}$, $\frac{\Delta\mu}{\Delta v_n}$, $\frac{\Delta\mu}{\Delta i_{dc}}$, $\frac{\Delta\mu}{\Delta\alpha}$ are obtained

3.3 AC current dynamic

As shown in Figure 10, the AC current is determined by the AC voltage and DC current. It can be expressed as:

$$L_c\begin{bmatrix}\frac{di_a}{dt}\\ \frac{di_b}{dt}\\ \frac{di_c}{dt}\end{bmatrix}=\begin{bmatrix}S_{coma-a} & S_{coma-b} & S_{coma-c}\\ S_{comb-a} & S_{comb-b} & S_{comb-c}\\ S_{comc-a} & S_{comc-b} & S_{comc-c}\end{bmatrix}\begin{bmatrix}v_a\\ v_b\\ v_c\end{bmatrix}+L_c\begin{bmatrix}S_{coma-idc}\\ S_{comb-idc}\\ S_{comc-idc}\end{bmatrix}\frac{di_{dc}}{dt} \tag{35}$$

where the switching functions are given in (6) and (15).

Considering m=0 in (6) and m=1 and -1 in (15), (35) can be rewritten as:

$$L_c\begin{bmatrix}\frac{di_a}{dt}\\ \frac{di_b}{dt}\\ \frac{di_c}{dt}\end{bmatrix}=\begin{bmatrix}\frac{\mu}{\pi} & -\frac{\mu}{2\pi} & -\frac{\mu}{2\pi}\\ -\frac{\mu}{2\pi} & \frac{\mu}{\pi} & -\frac{\mu}{2\pi}\\ -\frac{\mu}{2\pi} & -\frac{\mu}{2\pi} & \frac{\mu}{\pi}\end{bmatrix}\begin{bmatrix}v_a\\ v_b\\ v_c\end{bmatrix}+L_c\begin{bmatrix}\frac{\sqrt{3}}{\pi}\left[\cos\left(\omega_0 t-\alpha\right)+\cos\left(\omega_0 t-\mu-\alpha\right)\right]\\ \frac{\sqrt{3}}{\pi}\left[\cos\left(\omega_0 t-\alpha-\frac{2\pi}{3}\right)+\cos\left(\omega_0 t-\mu-\alpha-\frac{2\pi}{3}\right)\right]\\ \frac{\sqrt{3}}{\pi}\left[\cos\left(\omega_0 t-\alpha+\frac{2\pi}{3}\right)+\cos\left(\omega_0 t-\mu-\alpha+\frac{2\pi}{3}\right)\right]\end{bmatrix}\frac{di_{dc}}{dt} \tag{36}$$

Transferring (36) into pn frame, the voltage and current can be described as:

$$\frac{3}{2}L_c\begin{bmatrix}\frac{di_p}{dt}\\ \frac{di_n}{dt}\end{bmatrix}=\frac{3}{2}\begin{bmatrix}\frac{\mu}{\pi} & 0\\ 0 & \frac{\mu}{\pi}\end{bmatrix}\begin{bmatrix}v_p\\ v_n\end{bmatrix}+\frac{3\sqrt{3}}{2\pi}L_c\begin{bmatrix}e^{j(\omega_0 t-\alpha)}+e^{j(\omega_0 t-\alpha-\mu)}\\ e^{j(\omega_0 t+\alpha)}+e^{j(\omega_0 t+\alpha+\mu)}\end{bmatrix}\frac{di_{dc}}{dt} \tag{37}$$

The relationship between injection voltage v_p, v_n and the current i_{2p}, i_{2n} can be expressed as:

$$\begin{bmatrix}v_p\\ v_n\end{bmatrix}=\begin{bmatrix}L_c\frac{di_{2p}}{dt}\\ L_c\frac{di_{2n}}{dt}\end{bmatrix} \tag{38}$$

Substituting (38) into (37) yields:

$$\begin{bmatrix}\frac{di_p}{dt}\\ \frac{di_n}{dt}\end{bmatrix}=\begin{bmatrix}\frac{\mu}{\pi} & 0\\ 0 & \frac{\mu}{\pi}\end{bmatrix}\begin{bmatrix}\frac{di_{2p}}{dt}\\ \frac{di_{2n}}{dt}\end{bmatrix}+\frac{\sqrt{3}}{\pi}\begin{bmatrix}e^{j(\omega_0 t-\alpha)}+e^{j(\omega_0 t-\alpha-\mu)}\\ e^{j(\omega_0 t+\alpha)}+e^{j(\omega_0 t+\alpha+\mu)}\end{bmatrix}\frac{di_{dc}}{dt} \tag{39}$$

After the linearization of (39), the deviations $\frac{\Delta i_p}{\Delta v_p}$, $\frac{\Delta i_p}{\Delta v_n}$, $\frac{\Delta i_p}{\Delta i_{dc}}$, $\frac{\Delta i_p}{\Delta \alpha}$, $\frac{\Delta i_n}{\Delta v_p}$, $\frac{\Delta i_n}{\Delta v_n}$, $\frac{\Delta i_n}{\Delta i_{dc}}$, $\frac{\Delta i_n}{\Delta \alpha}$ can be derived.

3.4 The matrix of the small-signal model

Combining the deviations in Section 3.1-3.3, the small-signal model of an LCC converter can be expressed as:

$$\begin{bmatrix} \Delta i_p \\ \Delta i_n \\ \Delta v_{dc} \end{bmatrix} = \begin{bmatrix} K11 & K12 & K13 & K14 \\ K21 & K22 & K23 & K24 \\ K31 & K32 & K33 & K34 \end{bmatrix} \begin{bmatrix} \Delta v_p \\ \Delta v_n \\ \Delta i_{dc} \\ \Delta \alpha \end{bmatrix} \tag{40}$$

where

$$K11=K12=K21=K22=0, \quad K13=\frac{2\sqrt{3}}{\pi}\left(\frac{e^{j\alpha_0}+e^{j\delta_0}}{2}-\frac{\omega_0 A}{2s}\right), \quad K14=\frac{-2\sqrt{3}\omega_0 B}{\pi s}\left[I_{2p}e^{j(\alpha+\pi/6)}+jI_{2n}e^{j(\alpha+\pi/6)}\right],$$

$$K23=\frac{2\sqrt{3}}{\pi}\left(-\frac{je^{j\alpha_0}+je^{j\delta_0}}{2}-\frac{\omega_0 A}{2s}\right), \quad K24=\frac{-2\sqrt{3}\omega_0 A}{\pi s}\left[I_{2p}e^{j(\alpha+\pi/6)}+jI_{2n}e^{j(\alpha+\pi/6)}\right],$$

$$K31=\frac{\sqrt{3}}{2\pi}\left(e^{j\alpha_0}+e^{j\delta_0}\right)+\frac{\sqrt{3}}{2\pi}\left(je^{j\delta_0}V_p-je^{-j\delta_0}V_n\right)C, \quad K32=\frac{\sqrt{3}}{2\pi}\left(e^{-j\alpha_0}+e^{-j\delta_0}\right)+\frac{\sqrt{3}}{2\pi}\left(je^{j\delta_0}V_p-je^{-j\delta_0}V_n\right)D,$$

$$K33=L_c\left(1.5\mu_0-2\right)\left(s-j\omega_0\right)+\frac{\sqrt{3}}{2\pi}\left(je^{j\delta_0}V_p-je^{-j\delta_0}V_n\right)E, \quad K34=-\frac{\sqrt{3}}{2\pi}\left[\left(je^{j\delta_0}V_p-je^{-j\delta_0}V_n\right)F+\left(je^{j\alpha_0}V_p-je^{-j\alpha_0}V_n\right)\right].$$

$$A=(s-j\omega_0)e^{j\alpha_0}-j\omega_0 e^{j\alpha_0}-\left[(s-j\omega_0)e^{j\alpha_0}-j\omega_0 e^{j\alpha_0}\right]e^{-(s-j\omega_0)\mu_0/\omega_0},$$

$$B=j(s-j\omega_0)e^{j\alpha_0}+\omega_0 e^{j\alpha_0}-\left[j(s-j\omega_0)e^{j\alpha_0}+\omega_0 e^{j\alpha_0}\right]e^{-(s-j\omega_0)\mu_0/\omega_0},$$

$$C=\frac{\left(e^{j(4\pi/3+\delta_0)}-e^{-(s-j\omega_0)\mu_0/\omega_0}e^{j(4\pi/3+\alpha_0)}\right)}{\left(I_{2p}je^{j(4\pi/3+\delta_0)}+I_{2n}je^{j(2\pi/3+\delta_0)}\right)sL_c}, \quad D=\frac{\left(e^{j(2\pi/3+\delta_0)}-e^{-(s-j\omega_0)\mu_0/\omega_0}e^{j(2\pi/3+\alpha_0)}\right)}{\left(I_{2p}je^{j(4\pi/3+\delta_0)}+I_{2n}je^{j(2\pi/3+\delta_0)}\right)sL_c},$$

$$E=\frac{-0.5\left(1+e^{-(s-j\omega_0)\mu_0/\omega_0}\right)}{\left(I_{2p}je^{j(4\pi/3+\delta_0)}+I_{2n}je^{j(2\pi/3+\delta_0)}\right)},$$

$$F=\frac{e^{-(s-j\omega_0)\mu_0/\omega_0}\left(I_{2p}je^{j(4\pi/3+\delta_0)}-I_{2p}je^{j(4\pi/3+\alpha_0)}+I_{2n}je^{j(2\pi/3+\delta_0)}-I_{2n}je^{j(2\pi/3+\alpha_0)}\right)}{\left(I_{2p}je^{j(4\pi/3+\delta_0)}+I_{2n}je^{j(2\pi/3+\delta_0)}\right)}+e^{-(s-j\omega_0)\mu_0/\omega_0}.$$

Substituting the small-signal model of (14) and the transfer function of the control into (40), the AC admittance can be derived as:

$$\begin{bmatrix} \Delta i_p \\ \Delta i_n \end{bmatrix} = \begin{bmatrix} Y_{pp} & Y_{pn} \\ Y_{np} & Y_{nn} \end{bmatrix} \begin{bmatrix} \Delta v_p \\ \Delta v_n \end{bmatrix} \tag{41}$$

4 Impedance validation

The obtained LCC system impedances are compared to those measured from the time domain model using the frequency injection method. The detailed system parameters of the LCC HVDC system are given in Table 1. The validation is conducted with a 6-pulse converter first and then 12-pulse converter and systems including AC filters are studied.

To measure the admittance in the time-domain, positive-sequence and negative-sequence voltage perturbations are applied at the AC side. The amplitude and phase of the response voltage and current at the LCC terminal are obtained by FFT analysis, and then the admittances are calculated.

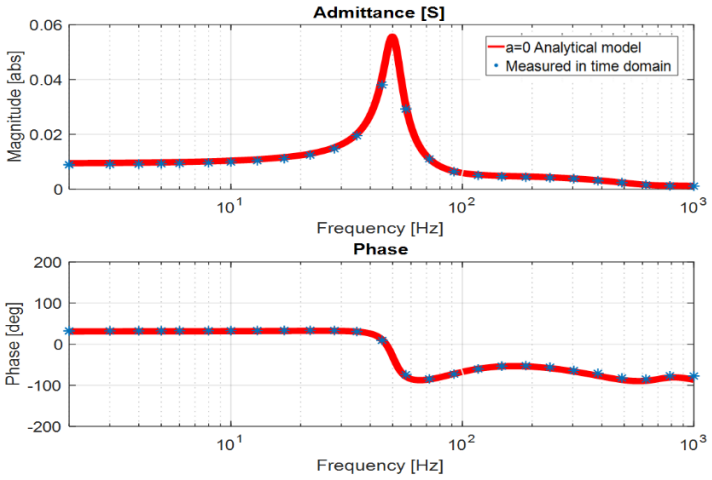
Table 1 Parameters of the tested LCC HVDC converter

Rated power	1000 MW
DC voltage	500 kV
AC network voltage	500 kV
Transformer rating	1250 MVA
Transformer leakage inductance	18%

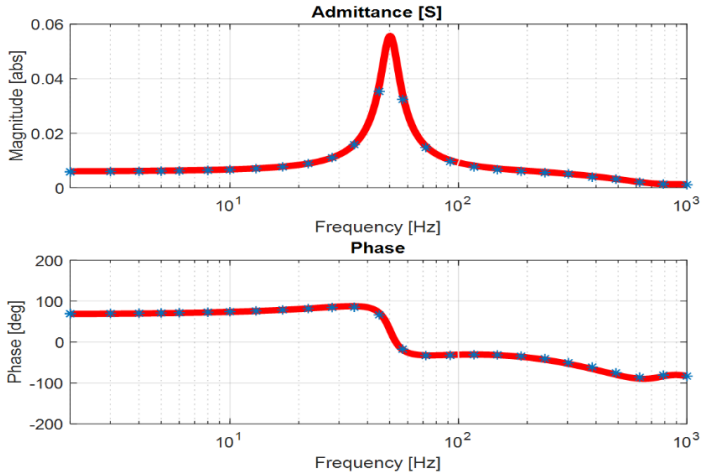
4.1 Impedance validation of six-pulse LCC converter

Figure 15 compares the measured admittance in time domain simulation and the calculated admittance using the developed analytical model for a six-pulse LCC converter. The firing angle is fixed at 0 degree and no control loop is included. Both the positive admittance Y_{pp} and negative admittance Y_{nn} calculated by the analytical model match well with the admittances measured in time-domain simulation, which indicates the correctness and accuracy of the developed model. It is noted that in the analytical model the interaction of the 11^{th} and 13^{th} harmonics with the fundamental frequency component is not included, while the obtained results are still highly accurate. Thus, the results also prove previous analysis that the interaction of the harmonics with the fundamental frequency disturbance is negligible due to the large frequency gaps.

The specific form of the small-signal admittance $\mathbf{Y}_{LCC}$ at the external LCC converter terminal can be represented as a 2 by 2 matrix as expressed in (41), in the same form as MMC admittance. This enables systems with LCC converters and VSCs/MMCs to be analysed together using the same method as previously used for studying system stability with multiple MMC converters.



(a) Positive admittance Y_{pp}



(b) Negative admittance Y_{nn}

Figure 15 Comparison of measured and calculated admittance

4.2 Open-loop admittance of a 12-pulse LCC converter

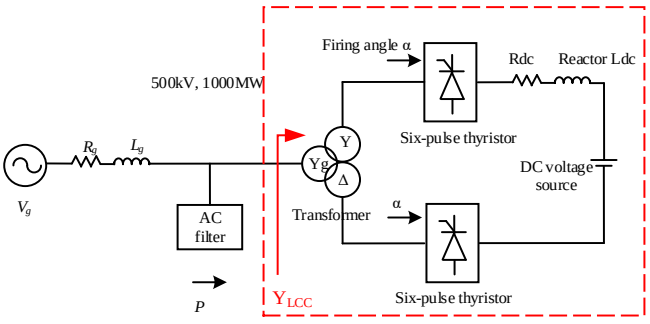
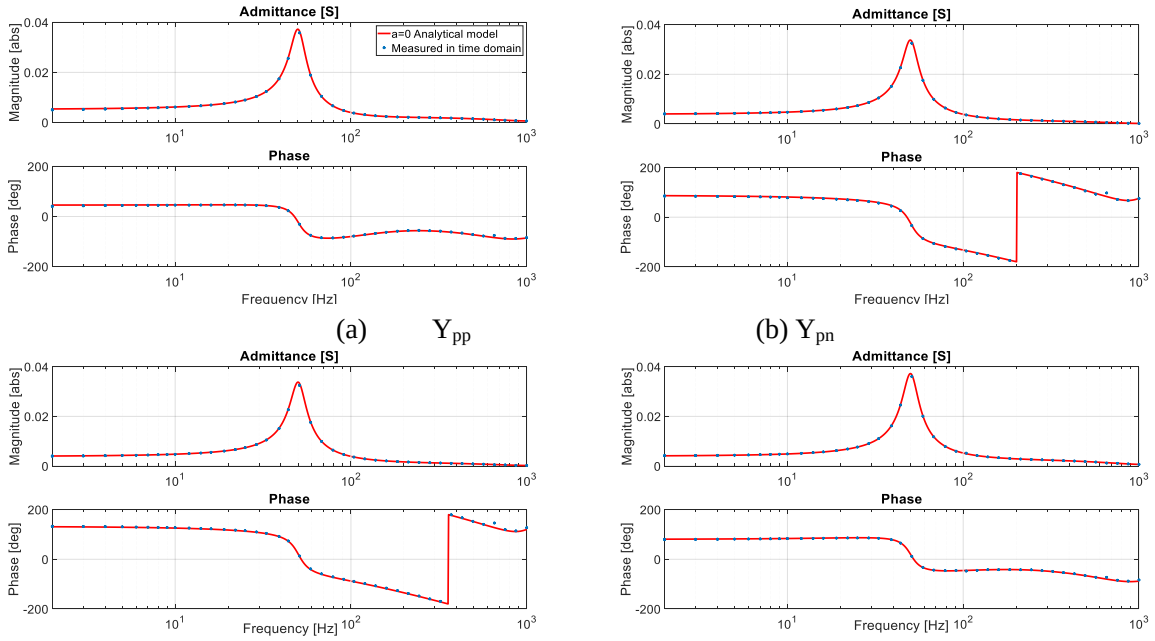


Figure 16 Twelve-pulse thyristor rectifier

One terminal of a 12-pulse thyristor rectifier is shown in Figure 16. The three-winding transformer has Y/Y/Δ connection to eliminate the 5th and 7th harmonic current, with ratios 9:5:5. Switched AC filters are used on the AC side, while the DC side circuit consists of a resistance R_{dc} (2.5Ω), a DC reactor L_{dc} (0.5H) and a DC voltage source.

4.2.1 Admittance validation

In the initial open-loop model with no controller included, the firing angle is fixed at α=0. The DC current I_{dc} is set to 1450 A by tuning the DC voltage source. The small-signal AC admittance of the LCC converter calculated based on the developed model is compared with the admittance measured in time-domain in Figure 17. As seen, the two results match well for all the 4 impedance elements, thus validate the adopted modelling approach. It also can be observed that the magnitudes of the coupling admittances Y_{pn} and Y_{np} are in the same order as the magnitudes of Y_{pp} and Y_{nn} indicating there is a strong coupling between the positive and negative components (while for MMC, the coupling is much weaker). Such strong coupling admittances can potentially affect the stability of the system and cannot be neglected for stability assessment.



(a) Y_{pp} (b) Y_{pn}

(c) Y_{np} (d) Y_{nn}

Figure 17 The admittances from the analytical model and time-domain simulation model

4.2.2 Different firing angles with constant I_{dc}

Changing the firing angle α and adjusting the DC voltage source to keep the DC current I_{dc} unchanged at 1450 A, the positive admittances are presented in Figure 18. It can be seen that the magnitude of the admittance is slightly lower while the phase is larger in the low-frequency range with a higher firing angle α. Again, the analytical results match well with the measured ones.

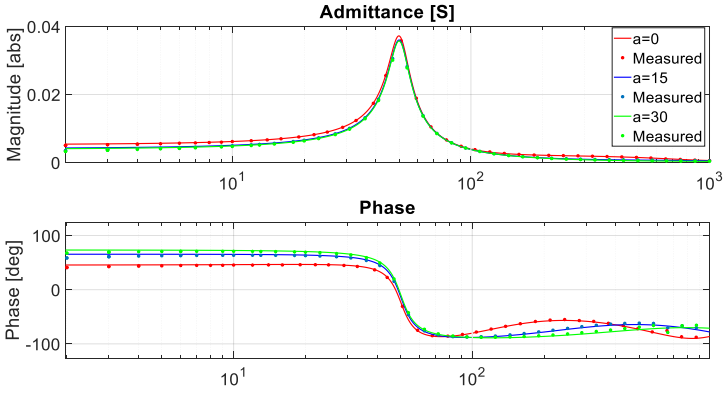


Figure 18 Positive admittance with different α

4.2.3 Different firing angles with constant V_{dc}

In this study, the firing angle is varied while the DC voltage remains unchanged. Consequently, the DC current varies with the change of the firing angle. Figure 19 compares the admittances for α=0 and I_{dc}=1470 A, with that of α=15 degrees and I_{dc}= 470 A. As can be seen, different firing angles and DC current result in a small difference in admittance magnitude though the impact on the phases is more significant.

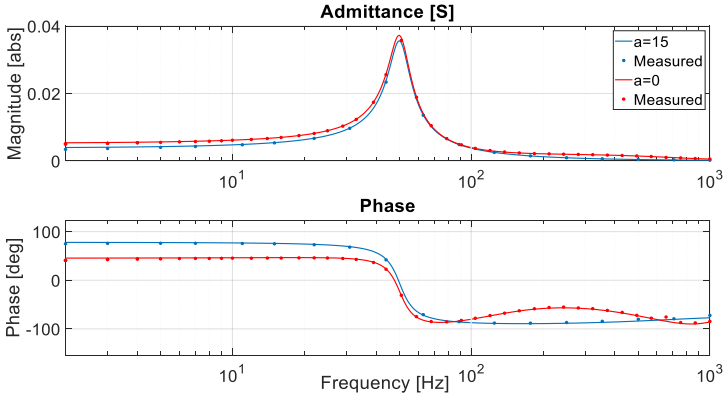


Figure 19 Positive admittance with different α

4.2.4 Different DC current with constant α

In this test, the firing angle is kept constant at α=15 degrees while the DC voltage source is adjusted to vary the DC current to be 470 A and 1450 A, respectively. The admittances are compared in Figure 20. The admittance magnitudes are largely the same while larger DC current results in relatively smaller phases.

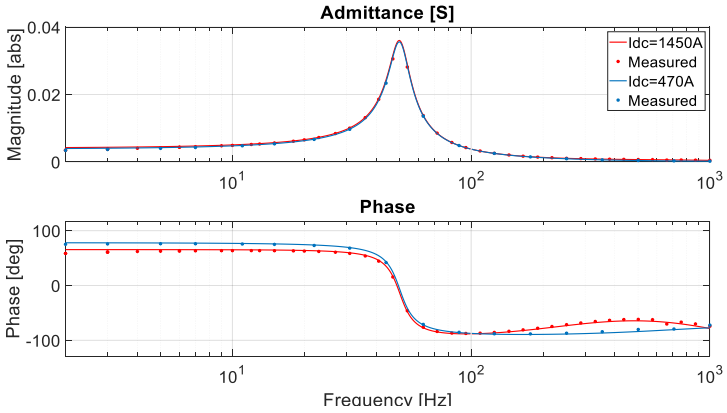


Figure 20 Positive admittance with different I_{dc}

4.2.5 Different DC reactance

The impact of DC reactance on the AC impedance of the LCC system is studied. With the same AC voltage, DC current and firing angle while halving the original DC reactance (L_{dc} reduced from 0.5 H to 0.25 H), the positive admittances are compared in Figure 21. It can be seen that DC reactance has a noticeable impact on the obtained AC side impedance, especially in the impedance magnitude. With lower DC reactance, the AC admittance becomes smaller. This also implies that AC admittance is affected by the DC side impedance so for a two-terminal LCC HVDC system, there can exist cross-coupling between the two converter terminals, as will be discussed in Section 4.5.

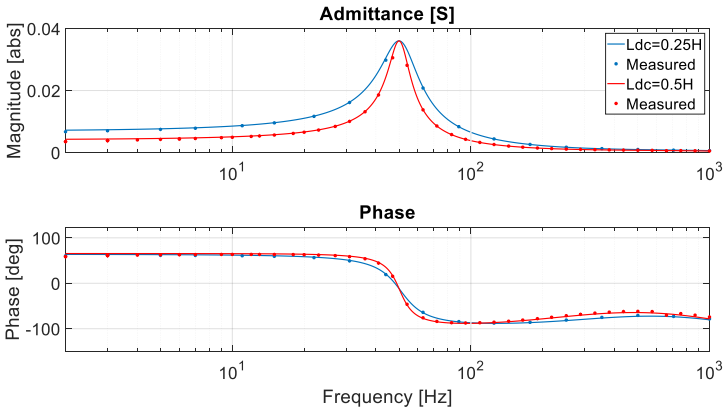


Figure 21 Positive admittance with different L_{dc}

4.3 LCC impedance with close loop control

In the previous studies, the LCC converter operates as an open-loop system with firing angle manually provided. The impedances of a closed-loop system with different controllers, e.g., DC voltage control, DC current control, are studied in this section.

4.3.1 DC current controller

The structure of the DC current controller is presented in Figure 22. The input is the measured DC current I_{dc}, and the PI controller is adopted to eliminate the error between the reference and measured current. Linearizing the DC current controller, the relationship between Δi_{dc} and $\Delta\alpha$ can be derived as

$$\Delta\alpha = K\left(K_p + \frac{K_i}{s}\right)\Delta i_{dc} \tag{42}$$

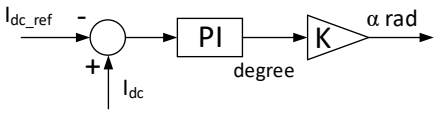
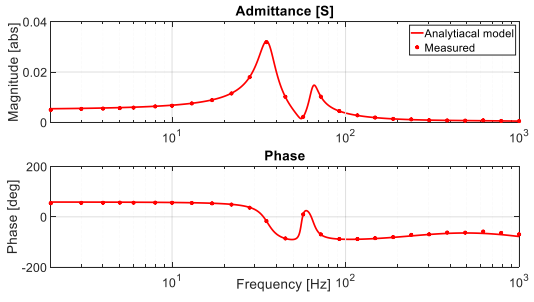
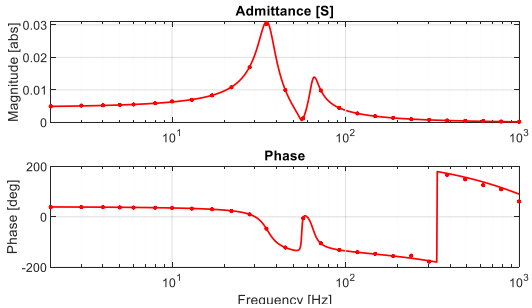


Figure 22 DC current controller

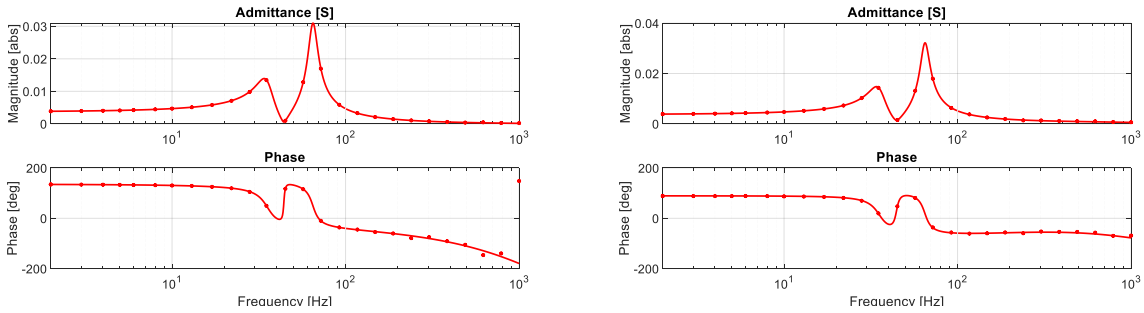
Substituting (42) into (40), the LCC admittance with DC current controller can be obtained. With a DC current reference of 1473 A (active power from the AC grid is 800 MW), the admittances are compared in Figure 23. With the current expressed in per unit term, the PI gains of the DC current controller are K_p=9.2 and K_i=3680. As seen, the calculated results match well with the measured ones from the time domain simulation model, validating the correctness of the modelling method.



(a) Y_{pp}



(b) Y_{pn}



(c) Y_{pp} (d) Y_{pn}

Figure 23 The admittance validation with DC current controller

Under the same operating state, the admittances with and without the DC current controller are compared in Figure 24. Compared to the open-loop admittances, it can be seen that the frequency of the impedance peaks with the DC current controller is shifted from 50 Hz (determined by the supply network frequency) to different frequencies of around 35 Hz and 70 Hz. At high frequencies, the admittances are largely identical so the DC current controller only affects the LCC admittance in the low-frequency range.

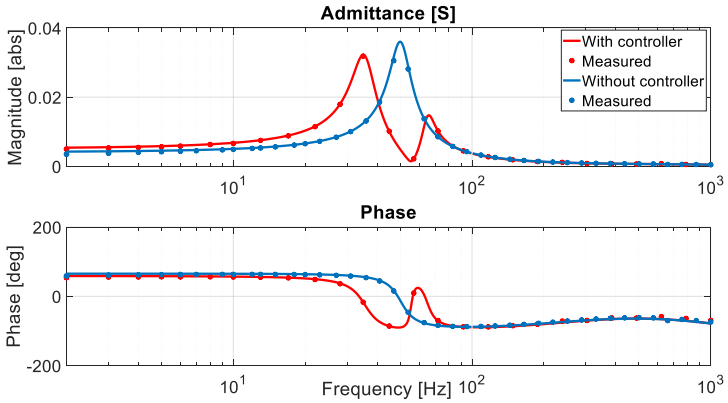


Figure 24 Comparison of positive admittances with and without DC current controller

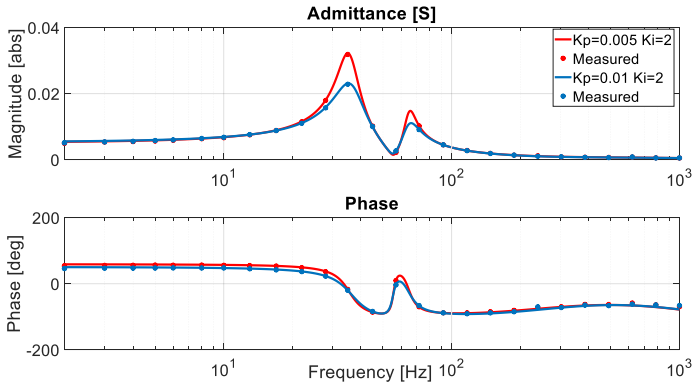


Figure 25 The positive admittance with different K_p

Figure 25 compares the LCC admittances with different DC current controller gain K_p. As can be seen, the main difference in the admittances are around the peak in the range of 20Hz to 70Hz, while larger K_p leads to smaller admittance.

4.3.2 PLL

In a LCC system, the PLL is used to generate ramp signals synchronized to the fundamental component of the positive-sequence voltage. The generated firing pulses can then be synchronized to the ramp signals. Thus, the relationship of the firing angle generated by the controller and the grid angle estimated by PLL are depicted in Figure 26.

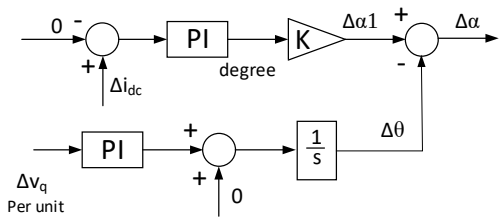


Figure 26 Small-signal model of PLL and the DC current controller

The transfer function of the PLL in dq frame is expressed as:

$$\Delta\theta = \frac{K_{pllp}s + K_{plli}}{V_d\left(s^2 + K_{pllp}s + K_{plli}\right)}\Delta v_q \tag{43}$$

Thus, the dynamic of the firing angle including the DC current controller $\Delta\alpha_1$ expressed in (42) and the PLL, is expressed as:

$$\Delta\alpha = \Delta\alpha_1 - \Delta\theta \tag{44}$$

The LCC admittance with DC current controller and PLL can be derived, as shown in Figure 27. As seen, the impact of having the PLL on the LCC admittance is relatively small. With different PLL bandwidths, Figure 28 compares the positive admittances. Again, it can be seen that the positive admittances with different control bandwidths are very close indicating limited impact of PLL on LCC admittance.

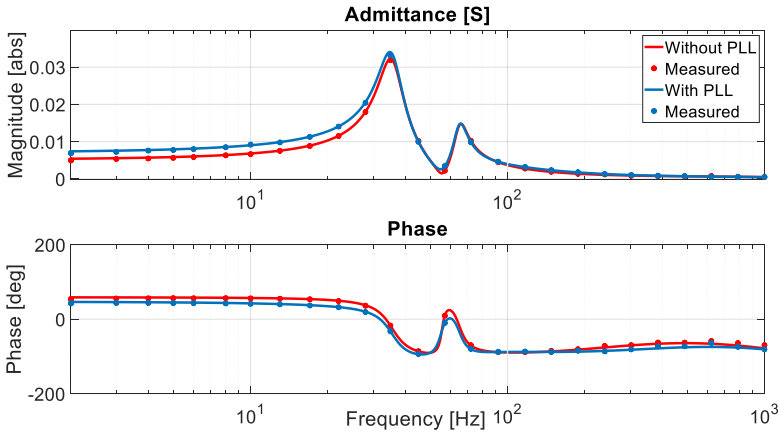


Figure 27 Positive admittance with PLL and without PLL

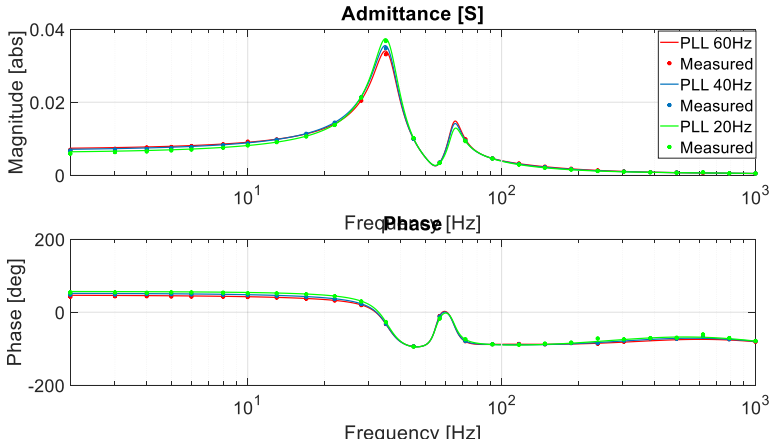


Figure 28 Positive admittance with different bandwidth

4.3.3 Admittance with different power and AC filters

Previous results show the LCC terminal admittances without the AC filters. In this section, the overall AC impedance of the LCC converter station is examined. AC filter design in the Cigre Benchmark model is adopted, and the structure and the parameters are shown in Figure 29. The parameters in the figure are those when the total reactive power capacity of the AC filter is 624MVar (used at full power transmission capacity). During lower active power transmission, the connected filters will be different to those shown in Figure 29.

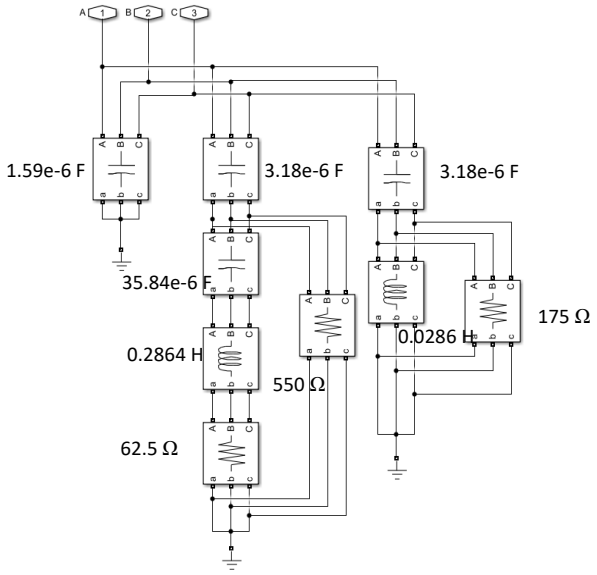


Figure 29 Structure of the AC filter (500kV AC voltage)

According to the structure of the AC filters, the admittance $\mathbf{Y}_{\text{filter}}$ in pn frame can be derived mathematically. As the AC filters are connected in parallel with the LCC, the overall admittance $\mathbf{Y}_{\text{ac}}$ for the LCC converter terminal can be expressed as:

$$\mathbf{Y}_{ac} = \mathbf{Y}_{LCC} + \mathbf{Y}_{filter} \tag{45}$$

Figure 30 shows the admittance with different transmission power and AC filters. When the active power is 1 GW, a total of 624 MVar of AC filters (as shown in Figure 29) are connected; while for 0.5 GW and 0.6 GW active power, the capacity of the connected AC filters is 312 MVar.

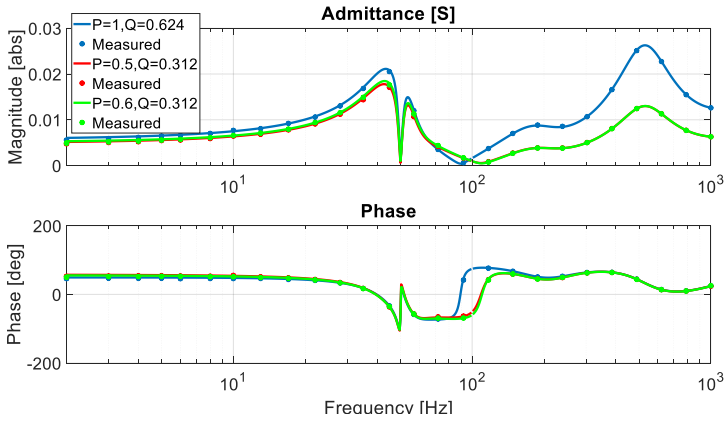


Figure 30 The admittance with different power and AC filters

From Figure 30, it can be seen that the admittance above 100 Hz is dominated by the AC filters, with the active power flow in the system has a small influence on the admittance at the low-frequency range. For a LCC HVDC system, the number of AC filters connected will be dependent on the active power transmission in order to keep the overall reactive power absorption of the LCC converter station within a certain limit. Thus, the overall LCC system impedance will be a function of transmitted active power.

4.4 LCC admittance in inverter mode

In this section, LCC admittance operating as an inverter is studied. Both open-loop and closed-loop systems are examined. Please note all the results presented in the followings sections include both the LCC converter and AC filters.

4.4.1 Admittance with open-loop

When the LCC is working as an inverter, the small-signal model is similar to the model of the LCC rectifier. Figure 31 compares the LCC impedance of the inverter with the impedance of the rectifier under open-loop. The two systems have the same DC and AC circuits while the firing angles are adjusted so they produce the same active power of 1 GW. The firing angle is 27.5 degrees for the rectifier and 141.3 degrees for the inverter. As seen, the admittances overlap indicating that LCC admittances are largely unaffected by operating as either an inverter or a rectifier.

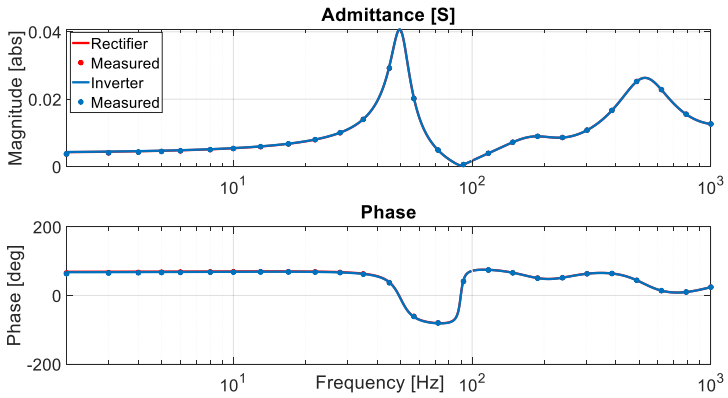


Figure 31 Comparison of open-loop admittances of LCC inverter and LCC rectifier

4.4.2 Admittance with DC current controller

The admittance of the inverter with DC current controller is compared to that of the rectifier with DC current controller as shown in Figure 32. For the two cases, the parameters of the DC current controller and PLL are identical. As shown, the admittances of the inverter and the rectifier with DC current controller show a noticeable difference at low frequencies, with rectifier admittance having higher resonant peaks around 30-60 Hz. The admittances are similar at frequencies higher than 90Hz, which are dominated by the AC filters.

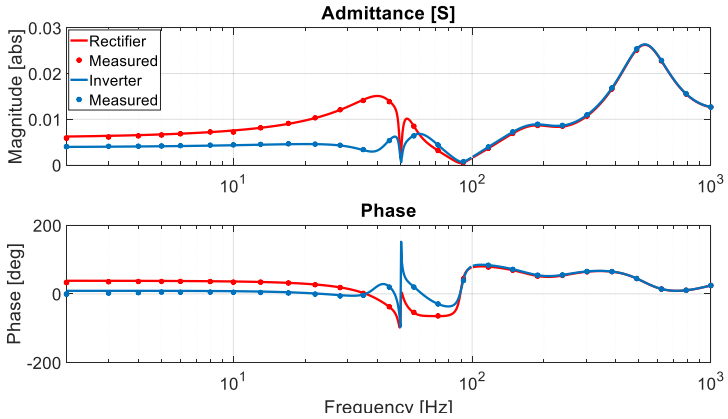


Figure 32 Admittances of LCC inverter and LCC rectifier with DC current controller

4.4.3 Admittance with DC voltage controller

The small-signal model of the DC voltage control and PLL is depicted in Figure 33. The measured DC voltage is compared with the DC voltage reference through a low pass filter, with a cut-off frequency of 15 Hz. The transfer function of the DC voltage controller is derived as:

$$\Delta\alpha_1 = -K\left(K_{pv} + \frac{K_{iv}}{s}\right)\Delta v_{dc} \tag{46}$$

where K_{pv} and K_{iv} are the PI controller gains.

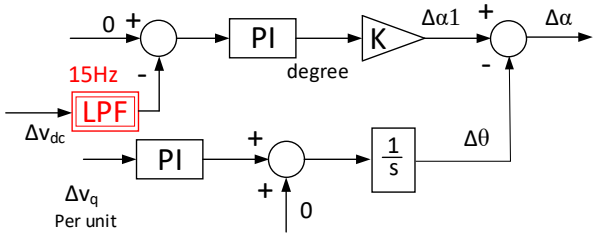


Figure 33 The small-signal model of the DC voltage control and PLL

Substituting (43), (44) and (46) into (40), the small-signal LCC admittance with DC voltage controller is obtained.

Figure 34 compares the inverter admittances with different control mode, i.e., DC voltage control and DC current control. With both voltage and current expressed in per unit terms, the parameters for the DC current controller are K_p= 20 and K_v=2000, while for the DC voltage controller, they are K_{pv}=35. and K_{iv}=2250. The active power for both cases is kept at 1 GW. As seen, with different control modes, the inverter

admittances appear different at low frequencies but remain largely the same at high frequencies due to the AC filters.

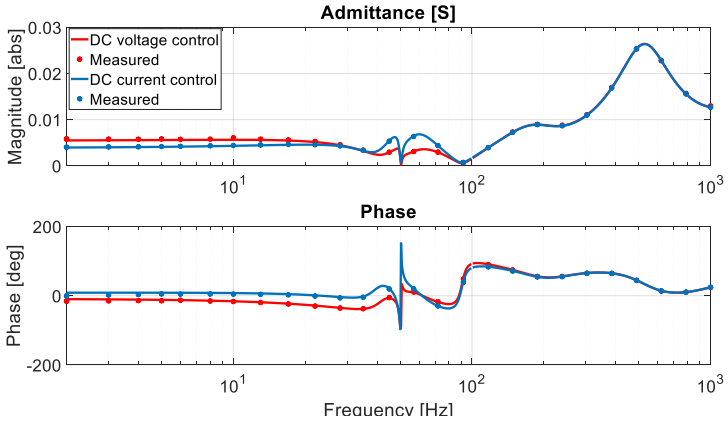


Figure 34 Inverter admittance with DC current control and DC voltage control

4.5 Admittance of LCC HVDC transmission system

The studied LCC HVDC transmission system is shown in Figure 35. The rectifier and the inverter are 12-pulse converters. The two converters are interconnected through a 0.5 Ω resistance and 0.5 H smoothing reactor in the model.

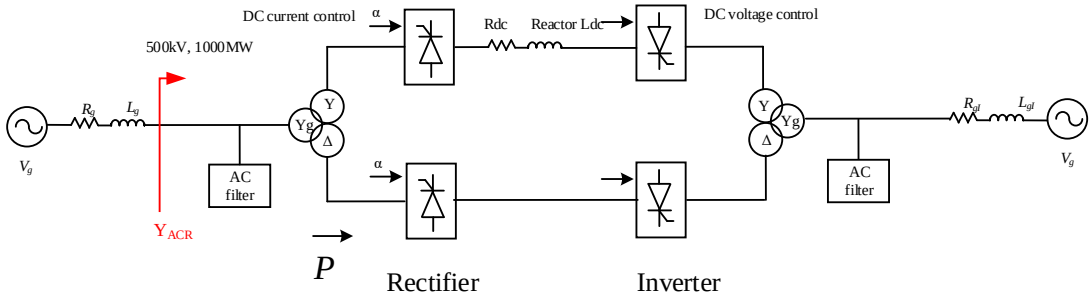


Figure 35 LCC HVDC system

4.5.1 DC impedance of LCC converter

From previous studies, it has shown that the DC side dynamics affect the admittance seen at the LCC AC side. When the two terminals are connected, the DC impedance of one converter will appear as part of the DC impedance seen by the other converter terminal. Therefore, to accurately calculate the AC impedance at each side, the DC impedances of the two converters must be obtained.

To consider the interaction between the rectifier and inverter, the LCC HVDC transmission system is divided into two parts, i.e., the rectifier side and inverter sider, as shown in Figure 36. At the DC terminals,

the inverter is equivalent to the frequency-dependent impedance Z_{eq} which will impact the AC admittance Y_{ACR} seen at the rectifier side. To assess the inverter DC impedance, an ideal current source is considered at the DC terminal since the rectifier controls the DC current, as shown in Figure 36. Thus, Z_{eq} can be determined by considering Δi_{dc} and Δv_{dc}.

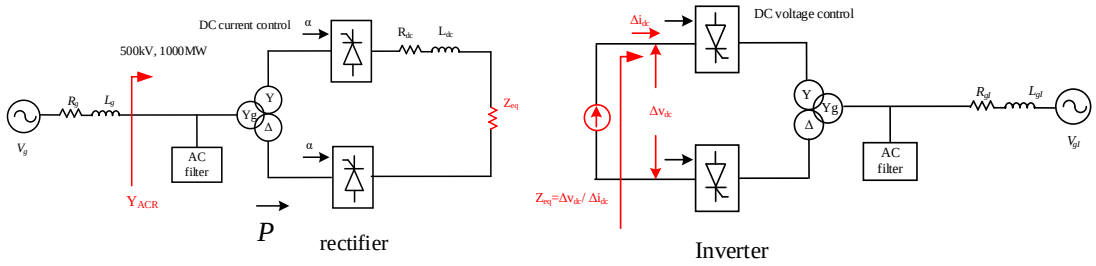


Figure 36 The two-converter equivalent circuits

For the inverter, the current disturbance Δi_p, Δi_n and the voltage disturbance Δv_p, Δv_n are determined by R_{gI}, L_{gI} (grid resistance and inductance) and AC filters, and can be denoted as:

$$\begin{bmatrix} \Delta v_p \\ \Delta v_n \end{bmatrix} = \begin{bmatrix} Z_{pp} & Z_{pn} \\ Z_{np} & Z_{nn} \end{bmatrix} \begin{bmatrix} \Delta i_p \\ \Delta i_n \end{bmatrix} \tag{47}$$

where Z_p and Z_n are derived according to the AC network on the inverter side.

According to (47) and (40), the equivalent DC impedance Z_{eq} of the inverter can be obtained. Thus, the DC impedance for the rectifier can be expressed as:

$$Z_{dc} = R_{dc} + sL_{dc} + Z_{eq} \tag{48}$$

Substituting (48) into (40), the admittance $\mathbf{Y}_{acR}$ seen at AC side of the rectifier can be obtained.

4.5.2 DC and AC admittance

As the AC network condition can potentially affect the DC impedance, so a system with a strong AC network is studied first. In this example, SCR for both the rectifier and inverter AC grids is 8.1. To simplify the analytical model, the AC filter at the inverter side is not included in the model. The equivalent DC impedances for the inverter are compared in Figure 37.

As can be seen, the calculated and measured DC impedances Z_{eq} at low-frequency region match well while there are noticeable differences at high frequencies. This is because in the analytical Z_{eq} calculation, the inverter side AC filters are not included, (while the real AC side impedance seen by the LCC converter includes both the network and the filters). However, the mismatch of inverter DC impedances Z_{eq} at high-frequency range is not expected to affect the calculated admittance $\mathbf{Y}_{acR}$ seen at the rectifier AC side since

the AC admittance at high frequencies is dominated by the rectifier AC filters. It can also see from Figure 37 that the controller adopted for inverter impacts the DC equivalent impedance Z_{eq}.

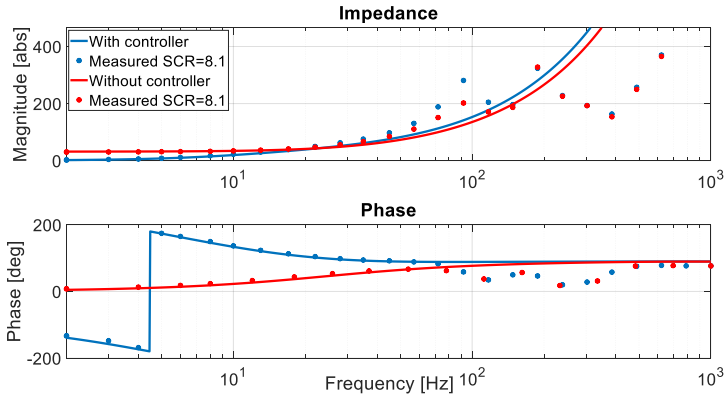


Figure 37 The equivalent DC impedance with and without controller for the inverter

Figure 38 compares the calculated and measured AC admittances at the rectifier side of the LCC HVDC link. As described, in the analytical model, the calculated DC impedance of the inverter is considered when calculating the rectifier AC impedance. From Figure 38, it can be seen that the calculated and measured AC impedances match well even the DC equivalent impedance is not accurate at high frequencies.

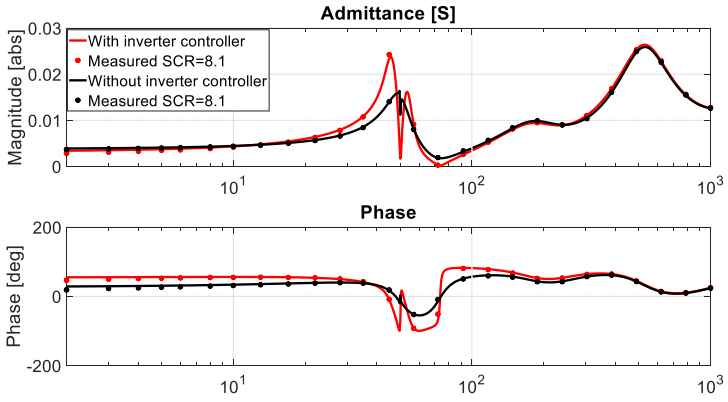


Figure 38 The AC admittance at rectifier side

4.5.3 Rectifier AC admittance of a LCC HVDC system

For different inverter network conditions, the rectifier AC impedances are obtained. When the SCR of the inverter side varies from 12, 8.1, 5 and 3.5 while the SCR of the rectifier side is unchanged at 8.1, the calculated and measured AC admittances at the rectifier are compared in Figure 39. As seen, the network strength at the inverter side affects the LCC AC impedance at rectifier terminal around the resonant peaks. As seen, for the system studied, significant differences in the impedance magnitude are observed when the

SCR at the inverter terminal changes from 5 to 3.5 while for higher SCR levels, the differences are much smaller. In addition, the phase of the LCC impedance moves to -180 degrees for lower SCR of 3.5, which is usually associated with less stable system.

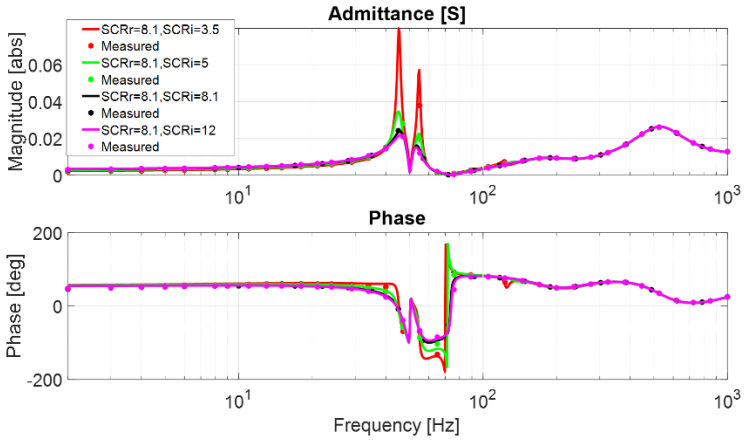


Figure 39 Rectifier AC admittance with different inverter network conditions

Thus, when assessing system stability involving LCC rectifier, it is necessary to consider the network condition (e.g., possible variation range) of the inverter terminal. As lower SCR at the inverter terminal likely leads to more critical rectifier impedance from stability consideration, primary focus thus should be given to the admittance of the system operating at low inverter SCR.

The concept of impedance representation is based on the principle that converter equivalent impedance at defined operating point and control is independent of the AC network for which the converter is connected to. To validate this concept, Figure 40 compares the measure rectifier impedances when the SCR of the rectifier AC network is changed from 8.1 to 2.8 for the same inverter SCR of 3.5, while the rectifier operating point remains unchanged. As can be seen, the variation of the rectifier AC network condition does not affect the obtained rectifier impedance, thus validating the general converter impedance representation concept. Please note, previous studies indicated the impact of the inverter network condition on the rectifier impedance.

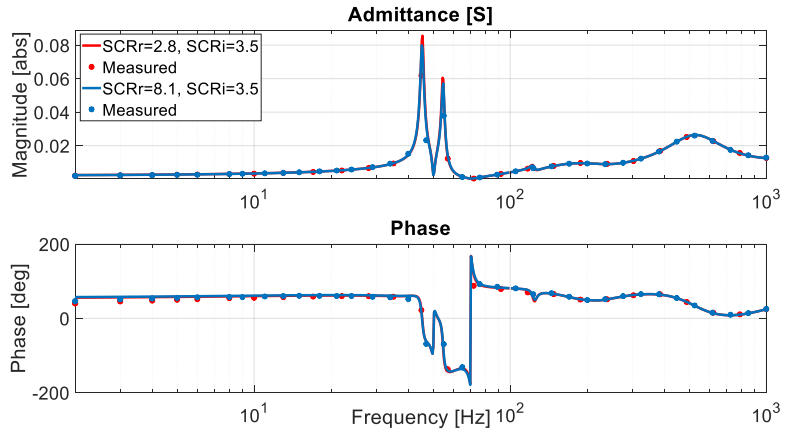


Figure 40 Rectifier AC admittance with different rectifier network conditions

4.5.4 Inverter AC admittance of a LCC HVDC system

Further investigations on the impact of different rectifier network conditions on the inverter AC impedance are also carried out. When the SCR of the rectifier side varies from 12, 8.1, 5 and 3.5 while the SCR of the inverter side is unchanged at 8.1, the calculated and measured inverter AC admittances are compared in Figure 41. As seen, the network strength at the rectifier side only has a small influence on the LCC inverter AC impedance, which is in contrast to the rectifier impedance change seen in Figure 39. Thus, when LCC inverter impedance is used for assessing system stability, typical rectifier network condition can be assumed.

Similar to Figure 40, the inverter AC admittances are compared in Figure 42 when the SCR of the inverter AC network is changed from 8.1 to 3.5 for the same rectifier SCR of 3.5, while the inverter operating point remains unchanged. As expected, the variation of the inverter AC network condition does not affect the obtained inverter impedance.

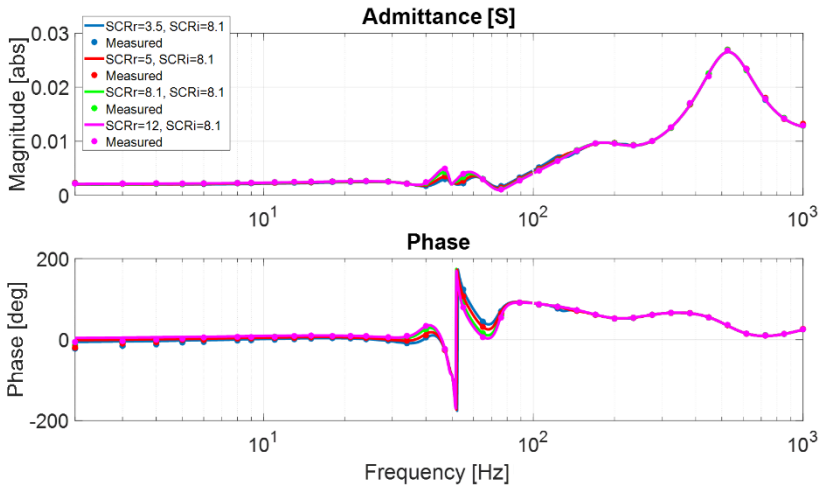


Figure 41 Inverter AC admittance with different rectifier network conditions

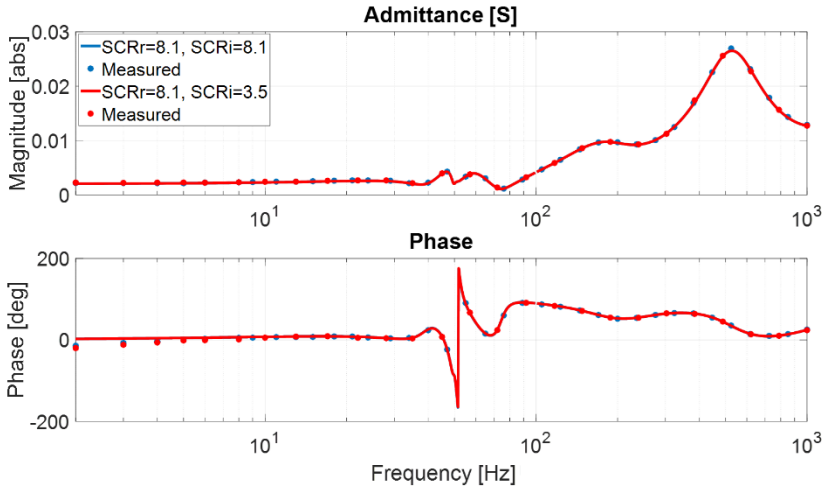


Figure 42 Inverter AC admittance with different inverter network conditions

5 Conclusions

This report describes the impedance modelling and validation of LCC HVDC systems. The fundamentals of impedance-based converter modelling have been introduced. The detailed mathematical expressions for modelling the LCC converter and LCC HVDC link have been derived. The small-signal impedances obtained from the developed analytical model have been validated using the measurement from the time-domain models. It has shown that:

- The admittance matrix of an LCC system can be represented by a 2x2 matrix, similar to other converter systems. Thus, a network that contains different converter technologies can be assessed by considering the impedance of each converter and the AC network.
- The operating point, such as power and firing angle, affects the impedance, though less significant than those observed in other converters like VSCs/MMCs.
- The control mode (e.g. DC current control, DC voltage control) has large impact on the converter admittance, while the controller parameters (PLL and controller gains etc.) only have a small impact on the converter admittance.
- AC filters significantly affect the overall impedance especially at the higher frequency range. Thus, the overall impedance of an LCC HVDC converter terminal at frequencies above 100 Hz is largely determined by the connected AC filters.
- For an LCC HVDC system, the AC impedance at one terminal is affected by the DC side impedance of the other terminal, while DC side impedance is affected by the converter control mode and the AC network condition (network strength and AC filters) for which the converter is connected to. The

study has shown that the main impact is on the AC impedance of the rectifier side during low network strength at the inverter terminal.

- When assessing system stability involving LCC systems, it is necessary to consider the network condition (e.g., possible variation range) of the other converter terminal, especially cases with the lowest possible SCR at the inverter terminal should be considered when studying the stability of the rectifier AC network.