Design and Validation of Pre-Insertion Resistor Rating for Mitigation of Zero Missing Phenomenon

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***Abstract*-This paper describes the design of pre-insertion resistor (PIR) for mitigation of 'zero missing' phenomenon (ZMP) observed in circuit breakers where the current does not cross zero through the breaker contacts for a period of time. Consequently, the breaker phases cannot be opened during faults on the system. The assessment was carried out for a typical offshore wind farm. The onshore end is a Gas Insulated Substation (GIS), and there is a requirement to install the circuit breaker with a pre-insertion resistor (PIR) for mitigation of this phenomenon.**

The feasibility of PIR for the GIS circuit breaker is analysed to mitigate this phenomenon. There will be an optimal value of resistance where there is no ZMP. During operation of the PIR, the value of resistance does not remain fixed due to the heat generated. Furthermore, manufacturing tolerances can lead to a resistance value which is different to that specified. If the resistance is not properly designed, then even a 'few ohms' variation in PIR resistance could lead to ZMP, and therefore, a potential failure of the breaker during faults.

Considering the aforementioned aspects, the upper and lower band of resistance, along with pre-insertion time (PIT), is derived, based on an iterative procedure. The energy capability of the resistor bank is decided based on the PIT, with different faults.

The lower and upper bands of resistance of a PIR is then verified with different system operating scenarios. The system is further analysed with the equipment tolerances included, and these tolerances may impact the durations. The minimum electrical insertion time is calculated based on all the above configurations, and at no stage does this lead to ZMP.

***Keywords*: Zero missing phenomenon, pre-insertion resistor, reactive compensation, export cables, circuit breaker, offshore wind farm.**

I. Introduction

Large generation of reactive power occurs in HVAC connected offshore windfarms due to the capacitance of the long export cable. To compensate the reactive power, shunt reactors are typically installed [1]. Due to their inductive characteristics, these can raise other technical challenges within the system. The current in the inductor should maintain its continuity and when it is connected at voltage zero, the current will have a DC component with an amplitude equal to the amplitude of the AC component. The duration of the DC component depends on the resistance of system components e.g. resistance of shunt reactor winding, external grid, export cable and transformers. If the inductor is connected at a peak voltage, no DC component will be present because the current will be zero at that moment. The capacitive current of the export cable leads system voltage by 90^0, and inductive current of the shunt reactor lags by 90^0. If energised at voltage zero, both the inductive and capacitive currents are in phase opposition to each other and tend to cancel out. This leaves a DC current in the incoming breaker, with no zero crossing for a period of time. During this period it is not feasible to re-open the circuit breaker (e.g. if a fault in the cable exists) because the circuit breaker should find the current zero for an arc interruption. This can take a long time (sometimes seconds) to attain. Hence, it is called zero missing phenomenon (ZMP). There are different mitigation methods addressed in the literature for ZMP and the application of any particular method depends on the system conditions like operating voltage, cable length and location of the system [2]-[4].

Fig. 1 shows the current for the cable and shunt reactor in phase opposition. These two currents cancel each other out, leaving the DC component. The magnitude of DC component depends on the amount of compensation, where lower shunt compensation results in lower DC component. The ZMP can theoretically be avoided by limiting the compensation to less than 50%. However, this may increase transient overvoltages, and cause the need for a larger STATCOM / SVC for meeting grid code reactive capability requirements.

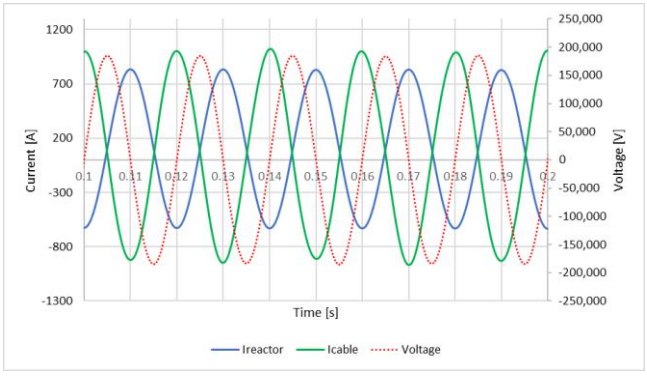

Fig. 1. Cable and reactor current in phase opposition

II. System Description & Modelling

The offshore transmission export cable in this example is 220kV HVAC, and includes reactive compensation equipment at the onshore and offshore substations rated at 120MVAr each. The export cable route length is approximately 80km. The maximum reactive power generated by the cable is

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282MVAr and the percentage compensation is calculated as 85%. The single line diagram modelled is shown in Fig. 2.

Proper modelling of the system components is important for the accurate calculation of voltages and currents in the simulation of the steady-state and transient. The range of frequencies of primary interest in a switching transients study vary from the fundamental power frequency up to about 10kHz [5]. The grid is represented by a voltage source of 400kV in series with a positive and zero sequence impedance, which are calculated from the short circuit current and X/R ratio.

The shunt reactor is represented by a non-linear inductance in series with resistance. The value of resistance is the predominant factor in determining the damping of DC component, therefore, it has to be calculated accurately. The resistance is calculated from full load copper loss, and the inductance is calculated from the rating of the shunt reactor.

Cables can be represented using either Bergeron model with parameters calculated at the switching frequency [5] or with multiple PI-sections. This representation is based on the fact that the resonance points occur at lower frequencies due to the high capacitance of the cable. In some cases, the frequency scan may contain multiple resonance points due to the cross bonding of the cable, which requires the use of frequency dependent cable model. Transformers are represented by their short circuit impedance and copper losses. The number of transformers operating in parallel have impact on DC component, therefore, net impedance of the transformer is less when they operate in parallel. Circuit breakers are modelled as ideal switches with infinite resistance (10MΩ) during an open condition and very low resistance (0.1mΩ) during a closed condition.

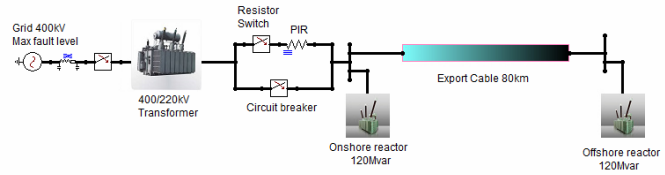

Fig. 2. Single line diagram of the modelled system

III. Effect of System Parameters on Zero Miss Duration

The duration of ZMP depends on various parameters of the system. It is important to determine the maximum zero miss duration (ZMD) before implementing any mitigation methods. A detailed explanation of the main factors impacting on ZMD are detailed in reference [6] and are summarised below.

A. Switching angle

The maximum ZMD is observed when the circuit breaker is switched at voltage zero (simultaneous or single pole). There is no ZMD observed for the circuit breaker when switched at voltage peak (single pole).

B. Grid short circuit strength

The damping of the DC component of the shunt reactor current during energisation, and during faults, depends upon positive and zero sequence impedance of the grid. The resistance for maximum fault level is less as compared to minimum fault level, which therefore leads to a slower damping of the DC component.

C. Type and location of fault

The zero-missing current is observed only in unfaulted phases of the circuit breaker. The current in the faulted phases crosses the zero point as it contains a large AC component due to the fault current. Hence, the faulted phases of the main breaker can interrupt the fault current but not the unfaulted phases. For compensation at both ends of the cable, the maximum ZMD is when there is a fault at the middle of the cable.

D. Degree of compensation

The maximum ZMD is at 100% compensation when the capacitive and inductive currents completely cancel each other out, and only the DC component remains. Above 100% compensation, inductive current is greater than capacitive current, and hence, only some AC component remains, resulting in a reduction of the ZMD. There is no ZMD below 50% compensation provided the shunt reactor has a minimum resistance to damp out the DC component.

IV. Pre-insertion Resistor

Circuit breakers with pre-insertion resistors (PIR) are often installed to damp out the transients during energisation [7]. There are basically two different PIR configurations: parallel and series PIR. In parallel PIR configuration (Fig. 3a), the resistor switch is in series with the resistor bank, and both are in parallel with the circuit breaker interrupter, where the interrupter operation follows the PIR switch operation. In a series PIR configuration (fig. 3b), the resistor switch is in series with the circuit breaker interrupter but in parallel with the resistor bank. Both the configurations are electrically the same for analysing the ZMP, however, the selection of a particular configuration depends on the manufacturer offering, space requirements, stresses imposed and the cost.

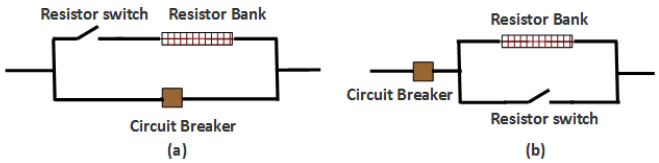

Fig. 3. PIR configuration: (a) Parallel PIR (b) Series PIR

IEC 62271-100 [8] specifies the different characteristic quantities of a circuit breaker with closing resistors as shown in Fig. 4. The closing time interval is defined as time between energising the closing circuit, the circuit-breaker being in the open position, and the instant when the contacts touch in all poles. The make time interval is the time between energising the closing circuit, the circuit-breaker being in the open

position, and the instant when the current begins to flow in the first pole. Pre-arcing time interval is the time between the initiation of current flow in the first pole during a closing operation, and the instant when the contacts touch in all poles for three-phase conditions, and the instant when the contacts touch in the arcing pole for single-phase conditions.

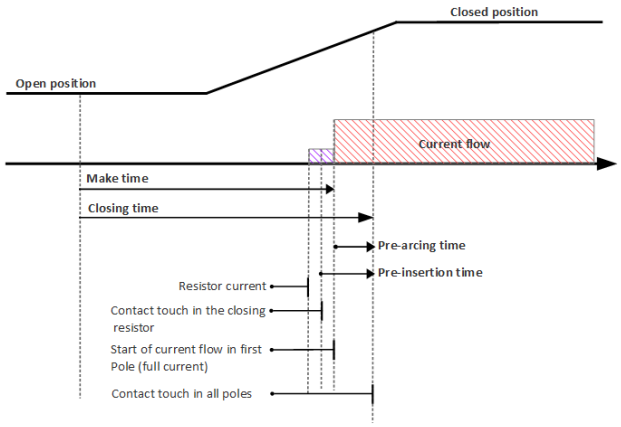

Fig. 4. Opening and closing operation of circuit-breaker with PIR

For a parallel PIR, PIT is defined as the interval of time during a closing operation in any one pole between the instant of contact touch of resistor switch, and the instant of contact touch in the main breaking unit of that pole. For circuit-breakers having series connected PIR, the PIT is defined as the interval of time between the instant of the last contact touch in any closing resistor element, and the instant of the last contact touch in any main breaking unit. From the above definition, the PIT for both the configurations are different for different phases. The PIT mentioned in this paper is the time for which the resistor in each pole is in circuit before the contact touching of the main breaking unit of that pole. It is important that a clear definition is used when supplying the design parameters to the circuit breaker manufacturer to avoid incorrect operation. Note that the term “main breaking unit” as used in [8], and “circuit breaker interrupter unit” are synonymously used in this paper.

The standard also specifies typical manufacturing tolerances for resistors to be considered. If a manufacturer has been selected, they should state the value of these tolerances. In addition, they should state the range of PIR insertion times which they can achieve (including time tolerances), as these are typically realised mechanically, and therefore depend on the physical design and ambient conditions.

V. Design of Pre-Insertion Resistor

The PIR value required to damp out the DC component in the shunt reactor can be obtained by solving a set of differential equations [9]. However, this method is considered overcomplicated and does not provide an allowable tolerance of the resistance for manufacturing purposes. The general method adopted in this paper is selection of a band of resistances for which there will be no ZMP, followed by selection of the optimal value from the average of the upper and lower permitted resistance.

One important objective is to determine the minimum PIT required. Reference [10] discusses about the effect of PIT for an overhead transmission line compensated with shunt reactors. There are some situations where the circuit breakers are designed to interrupt the short circuit currents with high value of DC component, which generally occurs near generating stations with high X/R ratio. Reference [11] has analysed such cases of the circuit breaker clearing the faults with delayed current zeros without necessitating a tripping delay. In many standard circuit breakers, the PIR PIT is 10ms [12]. However, different manufacturers may have different values depending on their design. In addition, this value can itself have a tolerance, and this must also be considered in the design process if it is available. The PIT, and the PIR values (and energy dissipation) which the manufacturer can achieve must then be considered together, and may lead to certain manufacturers being discounted from the procurement process if their offering cannot sufficiently resolve the ZMP on that particular site. However, if there is no manufacturer data available, then the process outlined in this paper can be followed to determine the basic requirements for tender documentation. It may then be required to repeat the study with the manufacturer data once it becomes available.

ZMP only poses a problem when there is a fault in the system. However, to verify the size of resistance required to damp the DC component completely, the system is first analysed under maximum grid fault level, without any fault on the system, as this is a simple procedure to determine the initial band. There will be an optimal range of PIR for which there is no ZMD. If the value is quite low, then it will not be sufficient to damp the DC component, and if the value is quite high then it acts as an open circuit and ZMD exists as soon as the main breaker contacts close.

The studies are commenced with an initial low value of PIT, with PIR switched simultaneously at voltage zero. As a starting step, the PIR value is varied in steps of 25Ω up to 375Ω with a PIT of 7ms. If there is ZMD observed through the circuit breaker contacts, the PIT is increased, and above procedure is repeated. For the studied system, the minimum PIT is determined as 10ms and the current through the circuit breaker interrupter for this case is shown in Fig. 5. The zoomed view of this plot is shown in Fig. 6. For 75Ω, the resistance is too low to damp out the DC component, and ZMD still exists. A lower limit of 100Ω is chosen, which also includes some margin. As the resistance is further increased, the value for which the current crosses zero becomes quite narrow, and the maximum resistance for which there is no ZMD is 300Ω. Note, however, that this resistance value is only applicable for the healthy system. For this value of resistance, the ZMP will still exist under certain fault conditions. This is because the magnitude of the DC component in the shunt reactor varies under fault. This is considered in the next section.

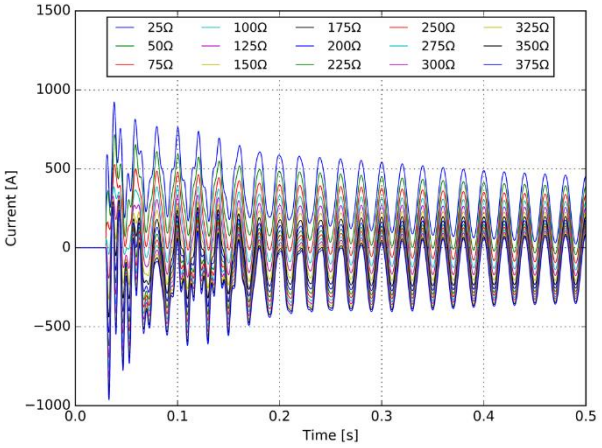

Fig. 5. Current through circuit breaker interrupter phase-A for different PIR values with PIT of 10ms (25Ω to 375Ω)

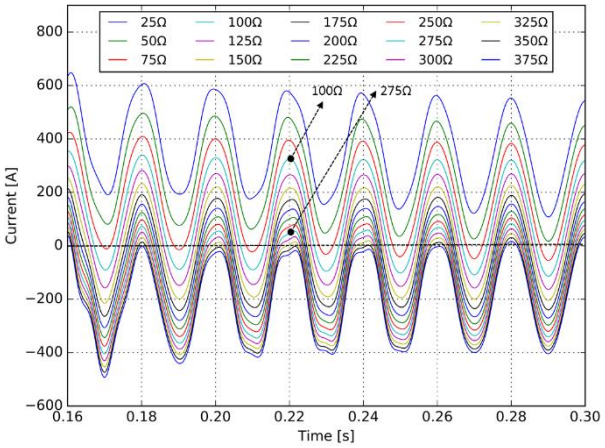

Fig. 6. Zoomed view of current through circuit breaker interrupter phase-A for different PIR values with PIT of 10ms (25Ω to 375Ω)

VI. Validation of Pre-Insertion Resistor with Faults

The selected band of resistance values are verified for different operating conditions and different faults on the system to ensure that ZMP does not occur in any of the cases. The lower value of 100Ω is determined to be suitable, however the upper values of 300Ω is not. Therefore, the upper value of resistance is further iterated and calculated under the range of faults. Different faults (single line to ground (SLG), double line to ground (LLG) & double line fault (LL)) are created at various positions in the export cable. The upper limit of resistance for which there is no ZMP is concluded to be 275Ω, which is 25Ω less than the case without fault. The range of allowable resistances chosen is therefore between 100Ω and 275Ω, with an optimal target value of 190Ω.

An example of the studies performed is given for a SLG-C fault at 50% of the length of the cable for breaker without PIR, with 100 Ω PIR and 275Ω PIR. For circuit breaker interrupter, the current through un-faulted phase-A and phase-B is shown in Fig. 7 & 8 respectively. it can be observed that the current crosses through zero with the inclusion of PIR resistance of 100 Ω (green curve) and 275Ω (red curve). For the circuit breaker without PIR it takes a period of time (>1s) to cross through zero (blue curve). The current through the faulted phase-C always crosses through zero due to high AC component as shown in Fig. 9.

For shunt reactor, un-faulted phase-A and phase-B the current always cross zero, however, the faulted phase-C will have a certain magnitude of DC component, and therefore, it does not necessarily cross through zero. This is not an issue, as the main breaker does have a zero crossing, and can therefore open and isolate the fault. Fig. 10 shows the current though the faulted phase-C of the shunt reactor for all three cases, where it can observed that there is a high magnitude of DC component without the PIR (blue curve) and this decay is fast when the PIR is connected (red and green curves). Fig. 11 shows the current through the phase-A of export cable, which always crosses through zero. In conclusion, there is no ZMP observed in the circuit breaker interrupter for PIR of 100Ω to 275Ω for all the fault types and locations considered.

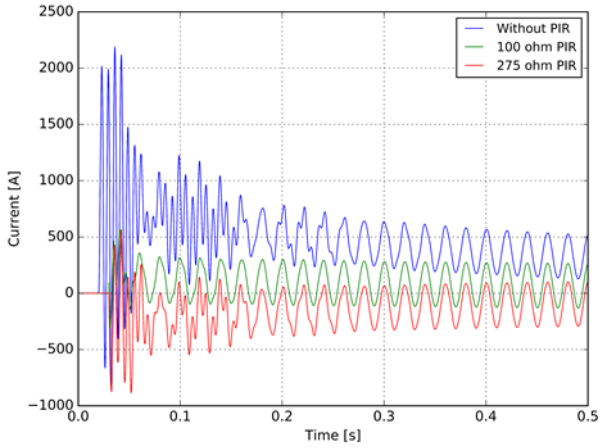

Fig. 7. Current through circuit breaker interrupter phase-A for SLG-C fault

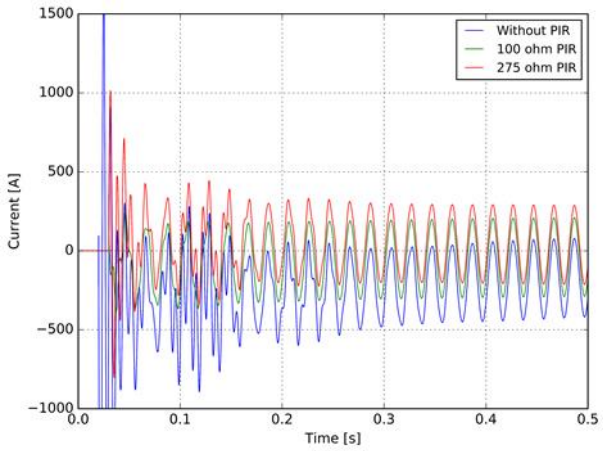

Fig. 8. Current through circuit breaker interrupter phase-B for SLG-C fault

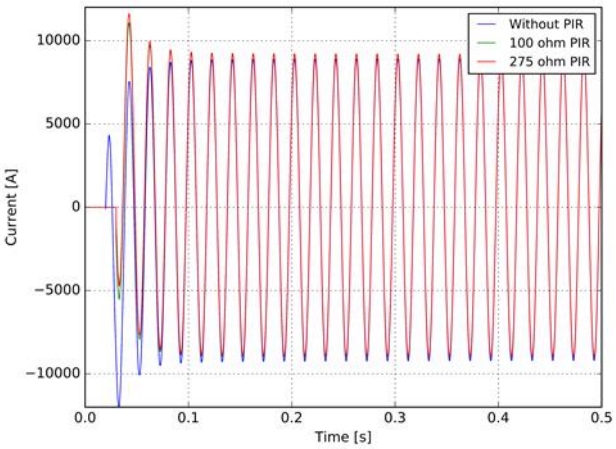

Fig. 9. Current through circuit breaker interrupter phase-C for SLG-C fault

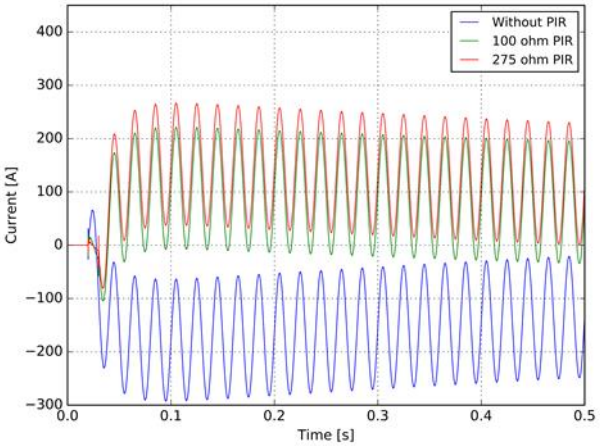

Fig. 10. Current through onshore shunt reactor phase-C for SLG-C fault

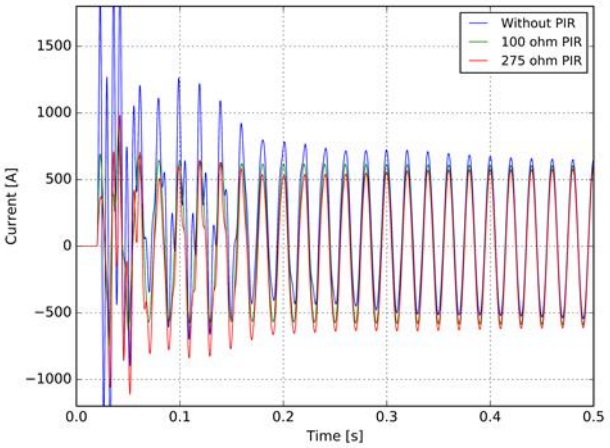

Fig. 11. Current through export cable phase-A for SLG-C fault

VII. Power and Energy Dissipation in Pre-Insertion Resistor

IEC 62271-100 [5] specifies that, for circuit-breakers fitted with closing resistors, the thermal capability of the closing resistors must be tested. The power and energy ratings are calculated for upper and lower values of PIR resistance for different faults, when considering a PIT of 7ms to 15ms. Please note that the minimum PIT selected from the analysis was 10ms, however, to verify the energy and power requirements, the plots are shown till 15ms for information. The energy and power requirements are lower without faults as shown in Fig. 12, as compared with faults as shown Fig. 13. The maximum energy requirement for 10ms PIT is 3.96MJ, with a 3-phase fault (LLLG). If there is a tolerance on the maximum PIT then the energy requirements have to be considered accordingly. For example, if the designed PIR has a PIT of 12ms with ±2ms tolerance, then the PIR energy requirements must be designed at 14ms with 5.71MJ (Fig. 13). Fig. 14 & 15 show the power requirements with, and without, faults for different PIT and PIR resistance. The maximum power is for three phase faults with the minimum PIR resistance value.

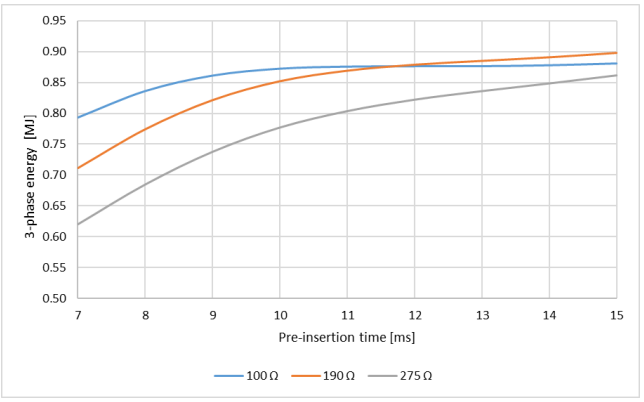

Fig. 12. Three phase energy dissipation in PIR without faults

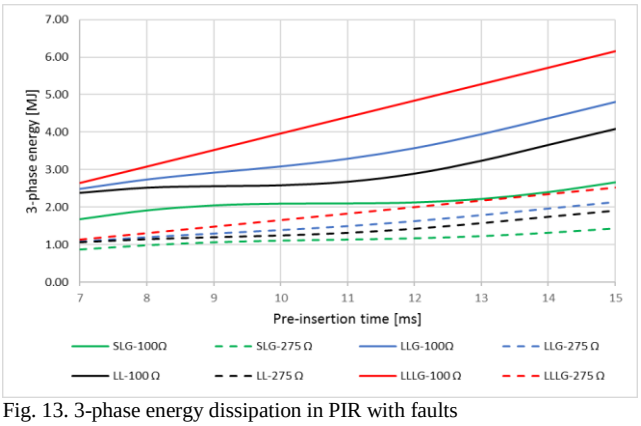

Fig. 13. 3-phase energy dissipation in PIR with faults

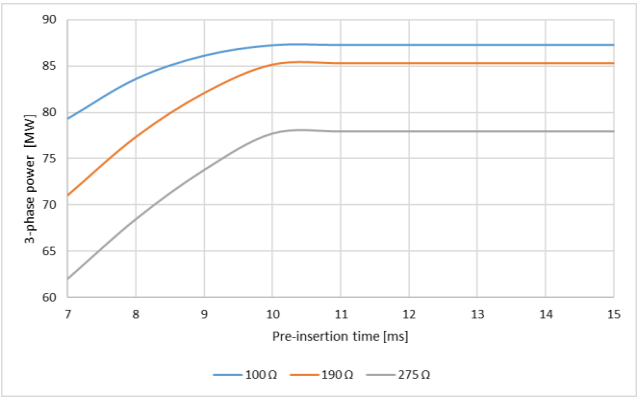

Fig. 14. 3-phase power dissipation in PIR without faults

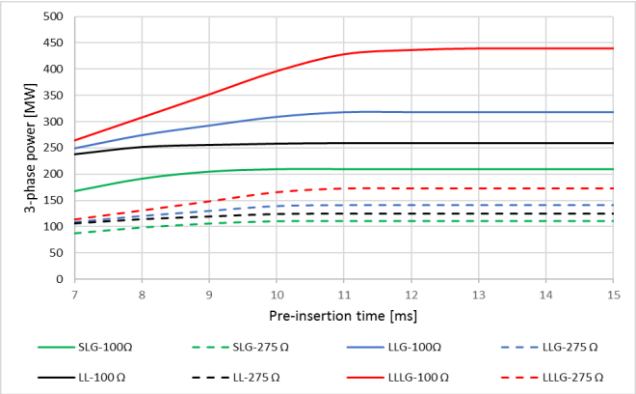

Fig. 15. 3-phase power dissipation in PIR with faults

VIII. Analysis of the System with Tolerances

The manufacturer will typically specify the tolerances for the main equipment at the design stage. It is important to consider these tolerances specifically for the export cable and shunt reactor ratings, in order to verify the ZMD with final designed values of PIR and PIT. Hence, the system is further analysed with tolerances included, where the export cable capacitance has been decreased by 5%, and the shunt reactor rating is increased by 5% (one at a time) to increase the degree of cable compensation (closer to 100% compensation means a longer duration ZMP). The onshore and offshore shunt reactors' nominal ratings are 120MVAr and after applying the +5% tolerance, the ratings are revised to 126MVar. The resistance, inductance and non-linear saturation characteristics of the shunt reactor are calculated for these increased ratings. The ZMD is verified for the system during different faults. The results show that there is no ZMP observed for a PIR resistance value between 100Ω and 275Ω, with PIT of 10ms. It can therefore be stated that there is no ZMP with the proposed PIR design, even when tolerances for the cable and shunt reactor are considered. However, note that it is essential that the PIR remains in place for at least 10ms. Therefore, if the PIT has a guaranteed tolerance of e.g. +/-2ms, then the default time should be 12ms.

IX. Conclusions

It can be observed that the PIR is very effective in mitigating the ZMP, provided the manufacturer can realise the required design. In summary, the high-level process described in this paper is as follows:

- Consider maximum fault level of the grid, and the circuit breaker switched simultaneously at voltage zero
- Start with a minimum value of PIT
- Determine the range of PIR which eliminate ZMP for healthy energisation without faults
- If the range is too small, or ZMP exists for all cases increase the PIT and repeat the above steps
- Confirm that the minimum and maximum resistance is sufficient for the system under various faults – refine the range if required
- Calculate optimum PIR value as an average of the upper and lower resistance band values
- Calculate the energy dissipation and power requirements for this range of resistance and an increased PIT (due to PIT tolerances)
- Provide the results as a specification for tender documentation or to the manufacturer including, optimum PIR value and permitted range, minimum PIT, and energy & power handling requirements for maximum PIT

Based on the information provided by different manufacturers, the PIR design mentioned in this paper can be realised for 220kV GIS and can be implemented for the system considered.

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