Four Considerations for High-Speed Digital Design Success

eBook

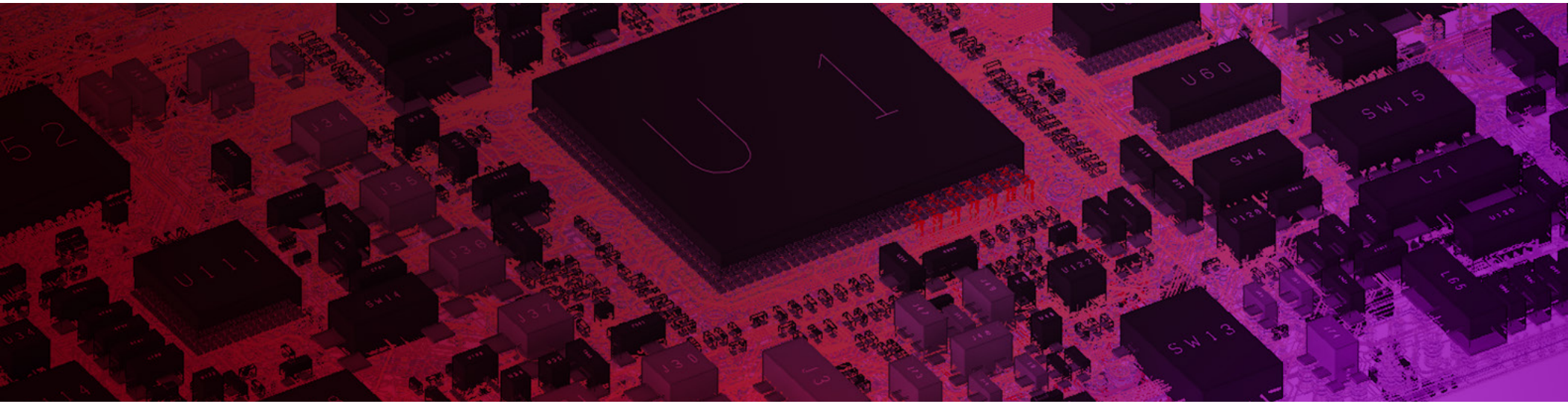
KEYSIGHT

As Complexity Increases, Holistic Design Is Necessary

High-speed digital standards are quickly evolving to keep pace with the data demand from emerging technologies such as 5G, the Internet of Things, artificial intelligence, virtual reality, and autonomous vehicles. Each generational change of high-speed computing standards provides new signaling features, faster data transfer rates, and smaller design margins. Faster speeds create new design challenges that require higher-accuracy simulation, new software tools, and more efficient workflows.

As a hardware engineer, your job is to design, verify, build, and test electronic products. Fail to adopt new design methodologies and you risk product failure caused by degradation of high-speed signals in your printed circuit board (PCB). You also risk project delays, a skyrocketing budget, or jeopardizing your stellar reputation.

Avoiding this dilemma requires new design tools and a holistic design methodology that connects the workflows of multiple disciplines. With this approach, you can design for the myriad interface standards, without increasing design and verification time. In this eBook, learn the four key considerations you need to know to realize successful, holistic high-speed digital designs.



Signal Integrity

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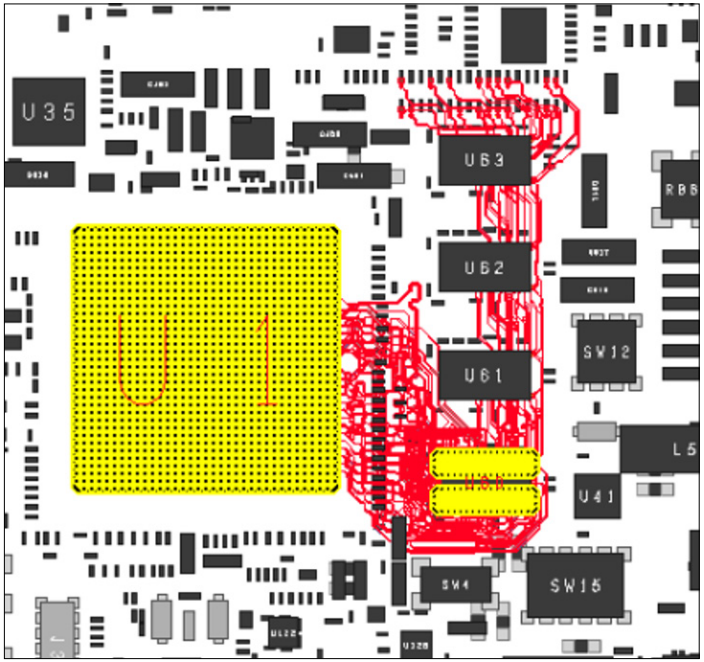
CONSIDERATION 1

Signal Integrity

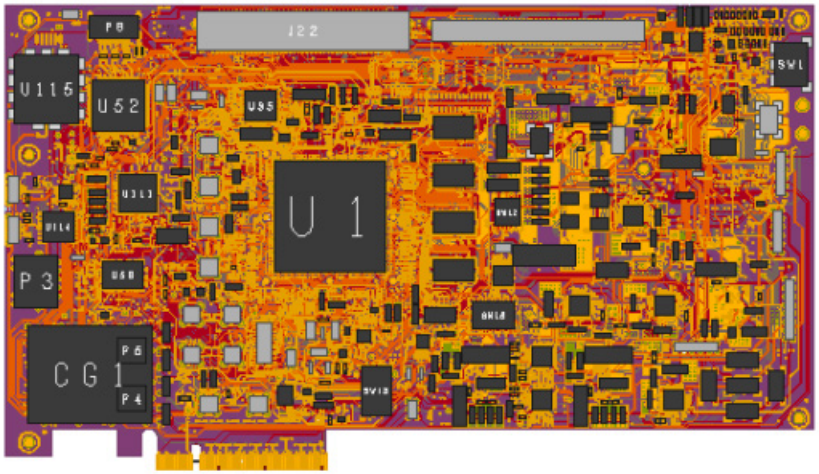
Signal Integrity Problems Cause Performance Issues

Signal integrity (the quality of an electrical signal) is all around us. In a digital communication channel, signal integrity analysis is the study of electrical signals as they traverse PCB traces, vias, connectors, and other components. Signal integrity problems can cause havoc for digital designs, including performance issues, lower yield, and possible failures in the field. These are costly problems as they often go undetected until late in the design and test cycle.



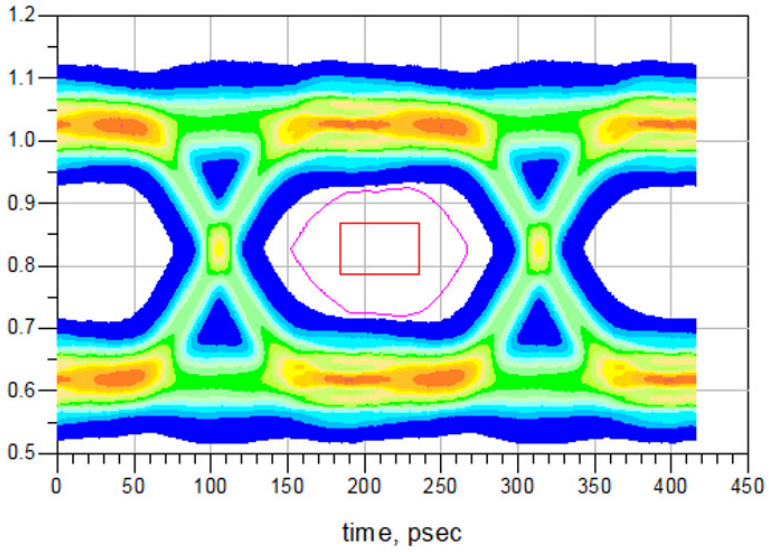
The best time to simulate a PCB for signal integrity is after layout and before fabrication. Taking the time to simulate becomes more important as speeds increase. There are now more factors that can lead to signal integrity problems. Common problems that can arise include reflections at the interconnects (mismatched impedances), electromagnetic coupling between the traces, and grounding issues. If not addressed, these problems can lead to signal distortion and attenuation.

Signal integrity analysis and simulation saves time and money in the long run because it reduces the risk of late-stage design failures and helps you maximize your design margin.



3 Steps to Understand Signal Integrity of a Digital Channel

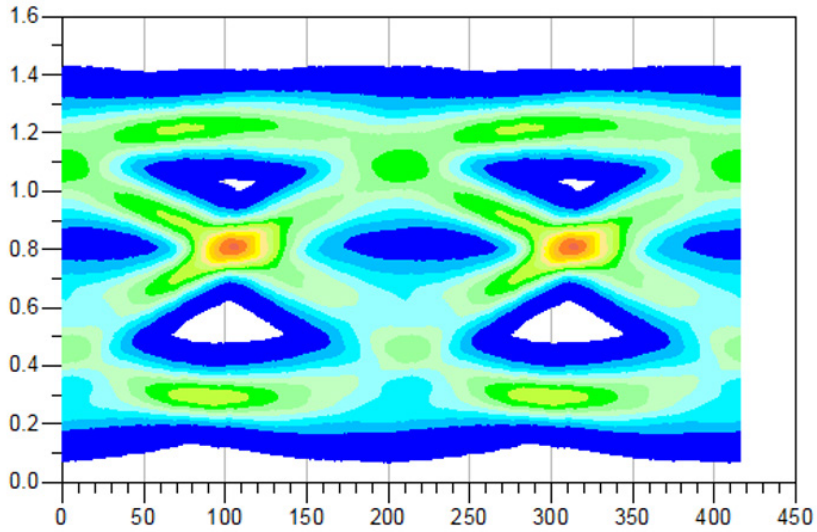
Ideally, you should consider signal integrity from the time you draw the schematic until the board passes final test. Testing your assumptions with simulation is the best way to verify the signal integrity of your channel. To do that, follow these three steps:



If the eye is open, the signal is good.

Step 1: Simulate the channel with an eye diagram

The signal travels from a transmitter to a receiver across the PCB. As it travels, traces, connectors, and cables introduce interference that degrades a signal in both amplitude and timing. An eye diagram can help you determine if the quality of the signal is still good enough when it reaches the receiver.



If the eye is closed, you have a signal integrity problem.

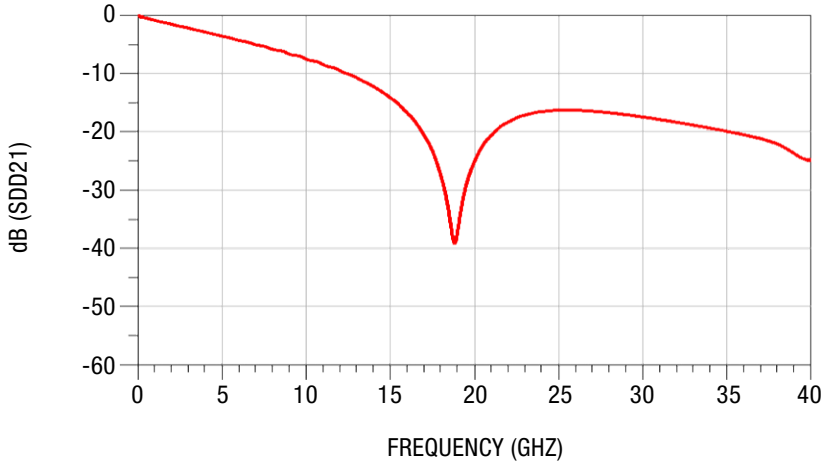
Step 2: Find the root cause of degradation

Once you discover a signal integrity problem, you can use two main analyses to determine its root cause in your design.

Mixed-mode S-parameters

Mixed-mode S-parameters tell you information about the frequency response of the channel.

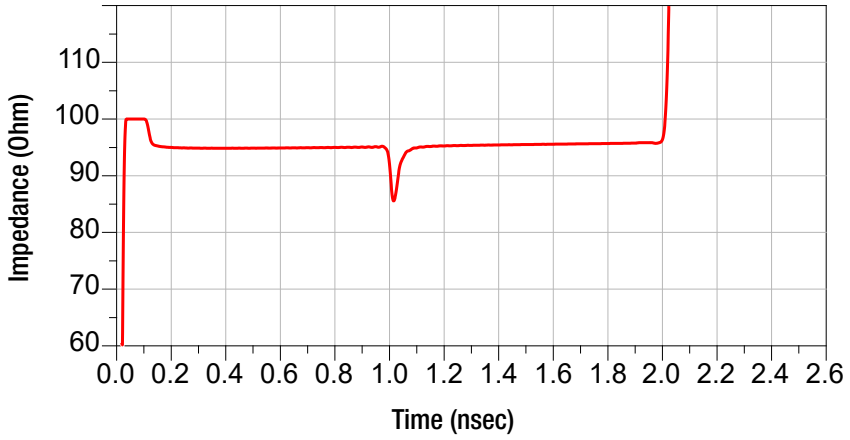
Looking at this graph of differential insertion loss, you would expect a linear response. Since there is a dip around 18 GHz, you know there is a signal integrity problem with one of your components at that frequency.



Time-domain reflectometry

Time-domain reflectometry uses reflected waveforms to provide information about the channel. It shows you spatial and timing information.

Notice a dip at 1.0 nsec? That dip tells you there is a signal integrity problem at that point in the channel.

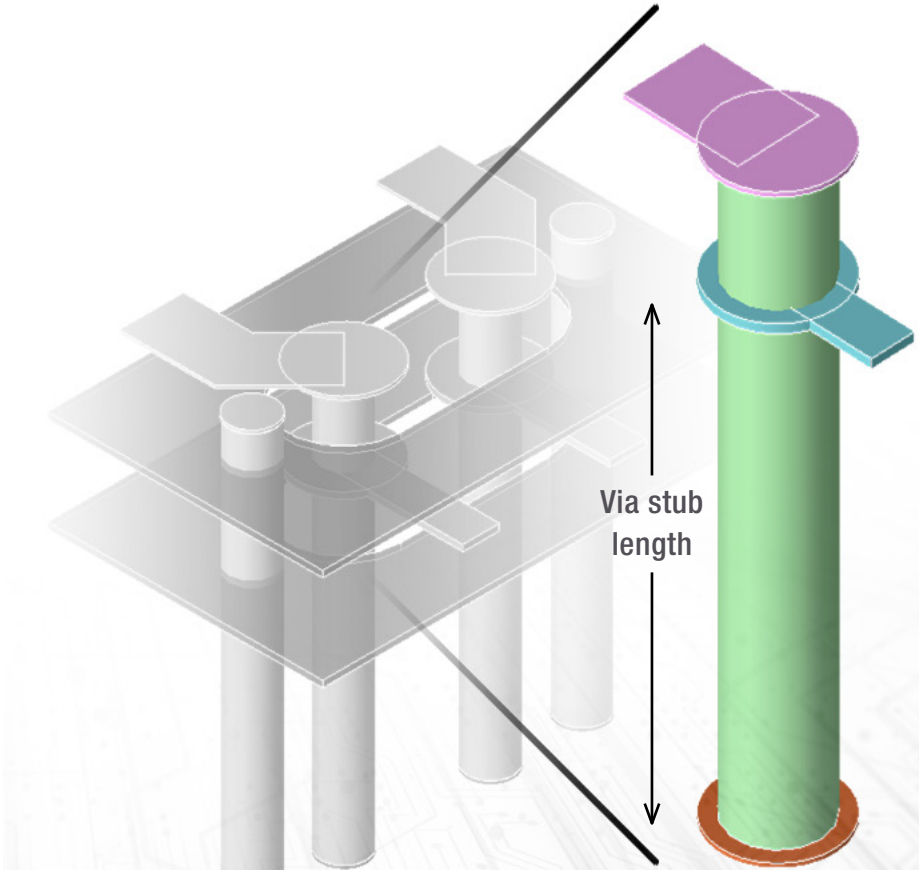


Step 3: Explore design solutions

Once you identify the root cause of your signal integrity problem, you need to consider what modifications you can make in your design.

One common cause is the length of a via stub. A via is an electrical connection between layers in the PCB. The via stub is the unused portion of the connector that can significantly degrade signal quality. Back drilling (removing the undesired stub section using a drill bit) can provide significant improvements in signal integrity.

After you make a design change, be sure to simulate the channel again to make sure your eye is open.



Want to Learn More?

Keysight University Course: Designing for Signal Integrity

CONSIDERATION 2

Power Integrity

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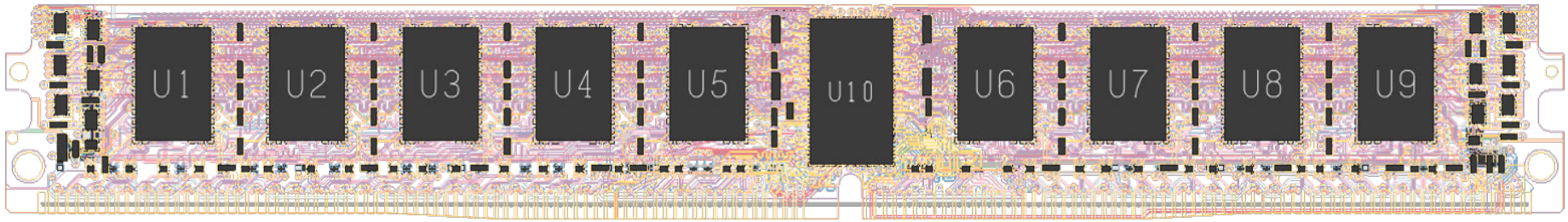
Predicting Power Integrity Early Is Paramount

Failing a compliance test at the end of the product design cycle is expensive. Retrofits with added filters and capacitors increase manufacturing cost. Design re-spins result in product delays and lost revenue. It is more effective to start early in the design phase to understand and mitigate potential power issues.

The objective of power integrity analysis is to ensure the drivers and receivers in your board get the voltage and current they need to operate correctly. To ensure power integrity, you want to avoid DC voltage drop (a measure of the voltage loss from current flowing through the resistance of the power and ground plane).



Early Design Exploration Is Key

Three main factors drive power integrity challenges and increase the impact of DC voltage drop.

1. **Higher device integration** – More integration creates denser routing, resulting in higher current density in the power network and more DC voltage drop.
2. **Lower supply voltages** – A 10% tolerance on 1 V is a tighter specification to meet than a 10% tolerance on a 1.2-V requirement, thus increasing the impact of voltage drop.
3. **Smaller form factors** – Less real estate on the PCB results in less space for wide power planes, causing DC voltage drop.

You can no longer afford to wait until after layout to perform power integrity analysis. Early design exploration is key to successful power delivery on high-speed digital boards.

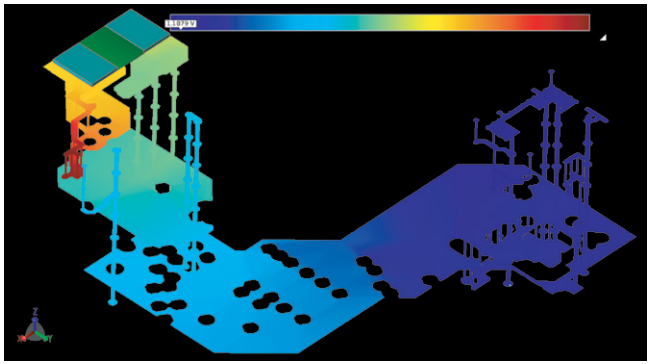
Two Key Analyses to Understand Power Integrity

Early simulation and analysis can help ensure the power integrity of your board. Be sure to consider these two analyses as part of your holistic high-speed digital design process.

Analysis 1: DC IR drop

When distributing power across a PCB, the voltage at the load may fail to meet necessary device specifications if the drop becomes excessive. DC IR drop analysis ensures the PCB traces and planes can handle the power supply requirements.

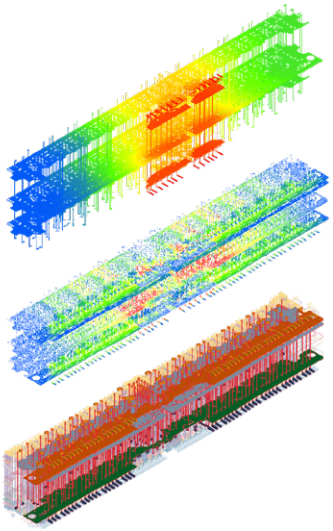
Using this analysis, you get visual feedback on exactly what the voltage distribution looks like for the selected power and ground nets. You can also view the current density to see how best to improve your design. Be sure to look at the placement of the power supply voltage regulator modules and their vias. Also consider the voids around the vias where the current is forced through narrow paths.



Analysis 2: AC impedance

While considering power integrity from a direct current (DC) perspective is important, it is equally important to consider it from an alternating current (AC) perspective. In the PDN, multiple integrated circuits act as sinks, each of which switches on and off at varied frequencies, hence AC. Decoupling capacitors can be used to store a local charge and minimize the effect of the changing current.

AC impedance analysis allows you to determine the optimal number of decoupling capacitors to minimize AC effects. With limited real estate on the board, optimizing the number of decoupling capacitors will save you money in manufacturing. Your optimal design will have the least number of decoupling capacitors, while still ensuring stability.



Voltage distribution

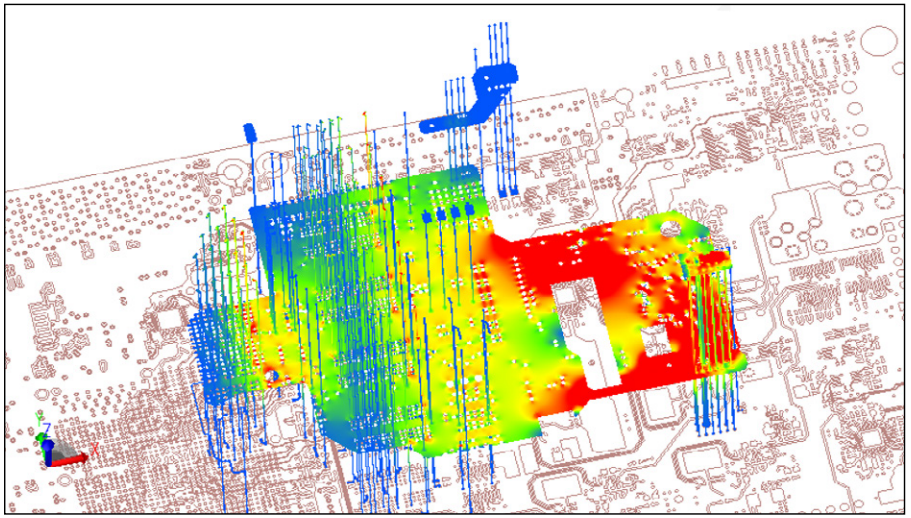
Current distribution

Return plane visualization

Flat Impedance Design Is the Goal

In the past, power integrity engineers used target impedance to ensure adequate power delivery across the frequency range they needed. Target impedance is the limit to the highest impedance for the PDN. If the target impedance stayed below this limit, then the designer believed power integrity would not be an issue.

In today's high-speed digital boards, target impedance is not enough. You must consider other noise sources affecting the board. The PDN impedance must be flat from DC to the highest-frequency components, not just below the target impedance. To ensure flat impedance, you can use the power supply's feedback loop for the low frequencies and decoupling capacitors for the middle and higher frequencies. You want an "optimally damped" design that avoids ripple and provides a fast settling time to large steps in current demand. The flat impedance method gives you both.

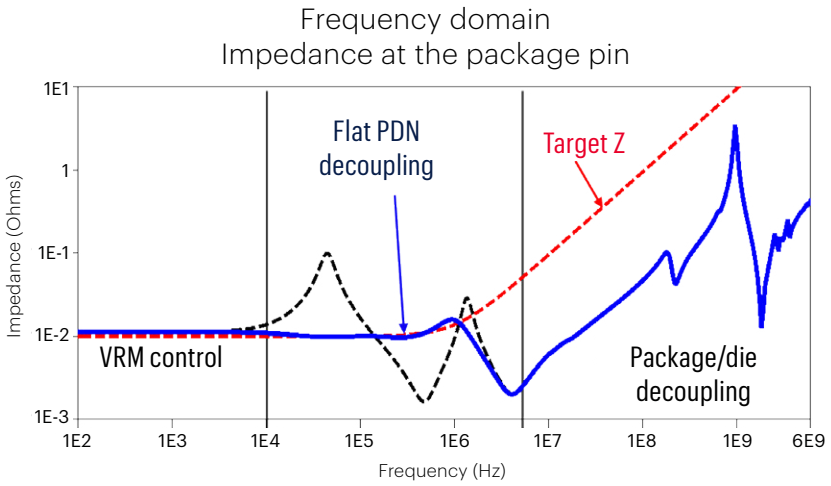


It takes only one rogue wave to kill a power distribution network. Flat impedance optimization before layout lowers the risk.

Optimize for Flat Impedance

Optimizing for flat impedance means using the minimum number of capacitors to achieve a flat impedance, while avoiding high resonances that can lead to rogue voltage waves. Reducing the number of capacitors also leads to higher reliability with fewer solder joints. Optimizing for flat impedance improves performance, lowers cost, and improves reliability.

Combining DC IR drop and AC impedance analysis, and designing for flat impedance provides a complete power integrity workflow. By addressing issues found in these analyses, you can cover the whole power integrity ecosystem, from generation to delivery at the load.



Want to Learn More?

- Video: Optimizing Decoupling Capacitors
- Video: Finding Power Delivery Noise Problems
- Video: Selecting a VRM
- Video: Measuring, Modeling, Simulating Capacitors and Inductors
- Video: DC-DC Converter Modeling and Simulation

CONSIDERATION 3

THERMAL EFFECTS

CONSIDERATION 3

Thermal Effect

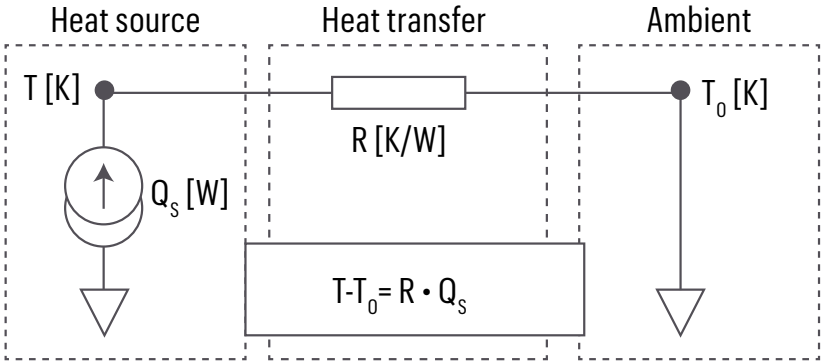
Boards are getting hotter

Designers are squeezing higher performance out of PCBs with more components in smaller spaces. Power densities are rising, and with them come high temperatures that can wreak havoc on conductors and dielectrics. Elevated temperatures, whether from voltage or environmental factors, affect thermal and electrical behavior, causing greater losses, erratic system performance, and even device failures.

Furthermore, high temperatures can cause reliability issues over time. Temperature cycles can cause via barrels to weaken and crack. Heat generation is always a factor for PCB design, but the demands of today's high-speed digital design boards are overwhelming traditional PCB heat management processes. Mitigating the effects of high temperatures has far-reaching implications, not just for performance and reliability of high-temperature PCBs, but also for weight, application size, cost, and power requirements.

As you design for thermal effects, ask yourself two questions:

1. Where are the heat sources?
2. How does the heat flow to the ambient?



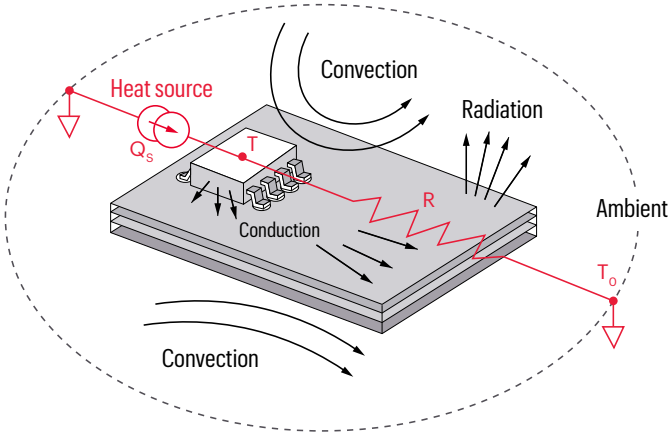
Where is the heat coming from?

Heat dissipates through one or more mechanisms: radiation, convection, and conduction. Keep all three in mind when deciding how to manage system and component temperatures.

1. **Radiation** – thermal energy transmitted through electromagnetic waves
2. **Convection** – thermal energy transitioning within a fluid
3. **Conduction** – thermal energy transferred between two objects by direct contact

Which via has the higher temperature?

It can be difficult to tell whether a via is undersized for the current passing through it. The temperature rise is dependent on the width of the traces attached to it. Also, the resistance of a trace increases with temperature. This makes it difficult to estimate the final temperature of a via with hand calculations. Instead, simulation analyses that take into account all the thermal effects are necessary to determine the final via temperature.

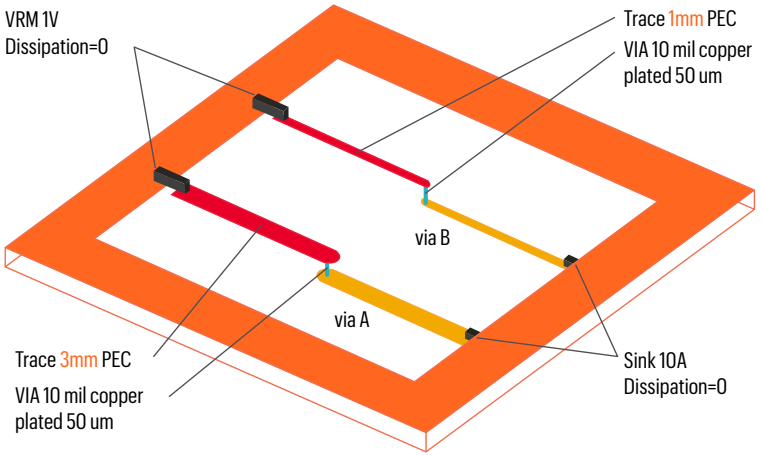


Test your assumptions – what do you think?

Given the same via, with the same ambient condition, which has the higher temperature?

- Via A with a 3 mm trace
- Via B with a 1 mm trace

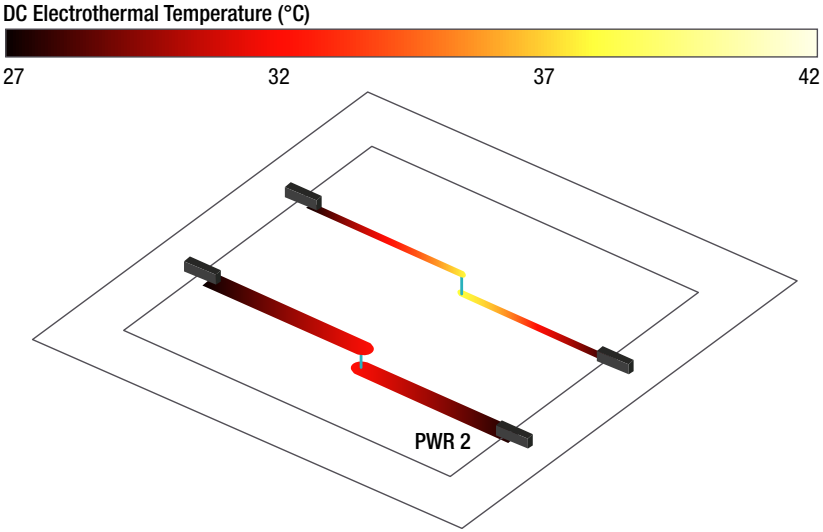
How much difference does the trace make in the temperature of the via?



Electrothermal Analysis More Accurately Predicts Temperatures

Answer: Via B

The one with a smaller trace is hotter. According to the electrothermal analysis, B is 42 °C and via A is 36 °C.



Why?

The metal trace connected to via A is wider, which improves the cooling effectiveness. But the answer is complicated. For every 10 °C change in temperature of the trace, we see a 4% change in resistance, which also increases the temperature of the via. The calculation needs to be done with an electrothermal simulator.

This is a simplified example. On high-speed digital boards, thermal heat dissipation and transfer are fairly complex. The cooling properties of the board depend on many factors, including available metal, material properties, component density and placement, cooling elements, and ambient conditions. All of these factors are interrelated. Electrothermal analysis is the only accurate way to predict thermal effects and prevent overheating.

Want to Learn More?

> Video: How to Set Up Electrothermal Simulation in ADS

CONSIDERATION 4

System Analysis

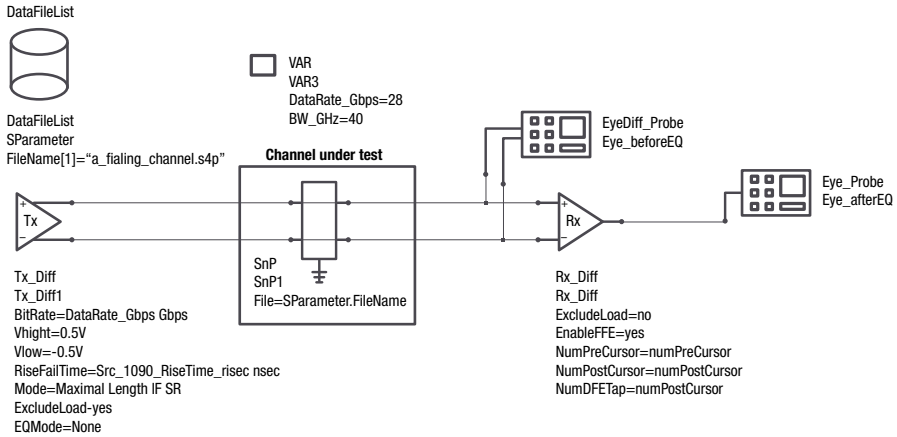
System Analysis

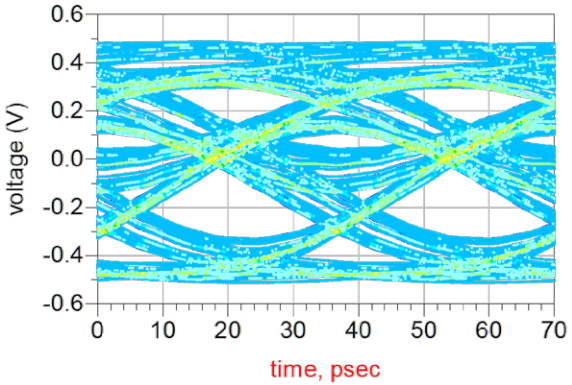
Increase confidence with channel simulation

New disruptive technologies spring forth from tough technical challenges. That is certainly the case for channel simulation, which became prevalent when transient simulation (SPICE) could not address the demands of modern high-speed digital boards.

Channel simulation enables rapid analysis of channels in high-speed serial and parallel communication links. In a typical scenario, a channel simulator processes million-bit patterns in minutes, allowing for accurate analysis of eye diagram properties, including density, width, height, bathtubs, and BER contours. The channel simulator accounts for intersymbol interference, random jitter, crosstalk, encoding, equalization, and other effects of interest to high-speed digital designers.

Using channel simulation increases your confidence that your entire high-speed digital board design will pass all specifications. It allows you to optimize complex systems where both PCB interconnects and equalization are working together.



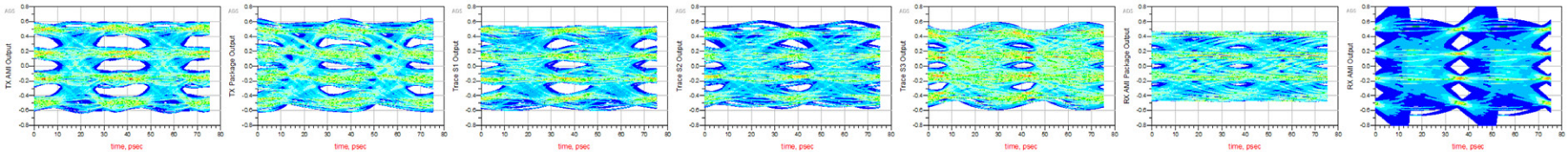


Two applications where channel simulation is necessary

Application 1: 400 gigabit Ethernet

The ever-increasing demand for a connected world with centralized data is driving Ethernet innovation. 400G Ethernet represents a significant and disruptive technological step for electrical interfaces on a PCB. Two modulation technologies enable 400G: non-return-to-zero and four-level pulse amplitude modulation (PAM4). While PAM4 enables higher data throughput, designs based on it are far more susceptible to noise because they pack four signal levels into an amplitude swing of two.

One way to handle the higher data throughput is using Input / Output Buffer Information Specification-Algorithmic Modeling Interface (IBIS-AMI) models. With IBIS-AMI models, you can accurately characterize transmitter and receiver performance, plus the models offer portability, IP protection, interoperability, and faster simulation. When considering IBIS-AMI models from a vendor, channel simulation is necessary. Without it, you cannot accurately simulate complex signal links with jitter, equalization, and clock and data recovery. A full channel simulation is essential to minimize intersymbol interference created by changes in impedance, particularly through vias.



Want to Learn More?

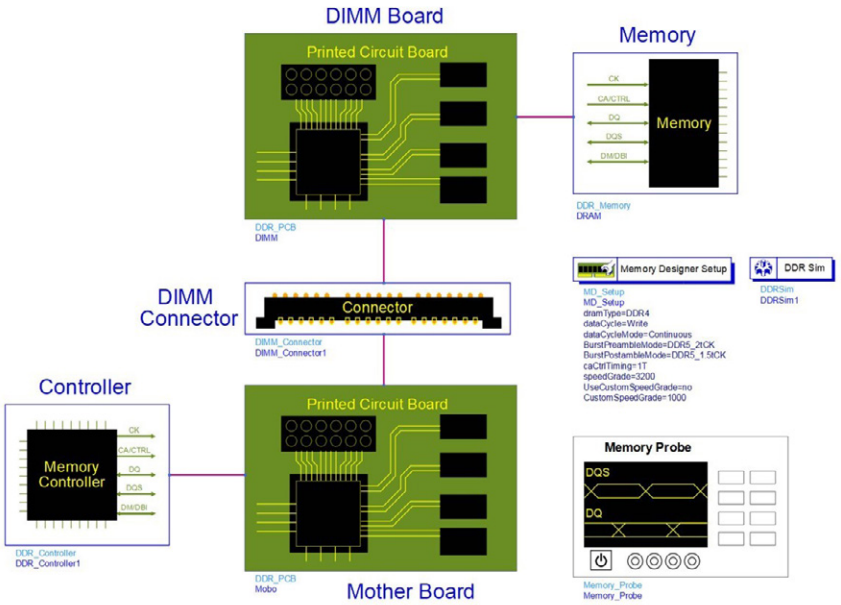
- Webinar: Designing for 400G–Evading the Pitfalls of 56 Gbaud PAM4
- Video: Build AMI Models Faster for DDR5/LPDDr5

Application 2: Double data rate memory

Double data rate (DDR) memory designs grow more complex with each new generation. Simulation and test configuration also grow in complexity, resulting in longer simulation and test setup times. The added complexity makes it harder to correlate simulation and test data, resulting in less confidence in designs, longer troubleshooting cycles, and missed delivery schedules.

Designers working on memory systems must contend with shrinking timing and voltage margins, as well as a complex list of compliance measurements, to ensure reliable operation. For the latest standards of DDR5 and LPDDR5, random jitter becomes more significant. Designers need to have confidence that their memory designs can pass receiver mask tests at ultra-low BERs.

Channel simulation can help you gain that confidence and model all the complexities of DDR5 and beyond. With shrinking margins, there is less room for error in memory designs. Channel simulation can quickly calculate corner cases.



Want to Learn More?

- Webinar: Designing for DDR4 and Beyond
- Video: DDR Simulation with PathWave ADS Memory Designer and SIPro
- Video: 3 Ways to Avoid Failing at DDR5 Speeds

SUMMARY

Learn More About High-Speed Digital Design

One of the biggest challenges in high-speed digital design is connecting the workflows of multiple disciplines. The four considerations we shared here are part of holistic high-speed digital design. But without a workflow that connects the results of one engineer to another, the design is not optimized efficiently. Keysight's integrated design and simulation software offers a high-speed digital workflow for fast, accurate, and optimized designs.

However you choose to move forward with your high-speed digital design, one thing is clear. Using the right design tool and a holistic design methodology that comprises the considerations outlined in this eBook are a smart way to quickly put you on the road to success.

For More Information ...

on how Keysight's PathWave Advanced Design System (ADS) can help you perform holistic high-speed digital design, or for a free trial, visit our website.

Keysight enables innovators to push the boundaries of engineering by quickly solving design, emulation, and test challenges to create the best product experiences. Start your innovation journey at www.keysight.com.