Lecture 3

Wafer Clean and Wet Processing

Recap Wafer Fabrication

- Czochralski (CZ) Method
- Float Zone (FZ) Method
- From Ingot to Wafer
- Gettering
- Silicon-on-Insulator (SOI)

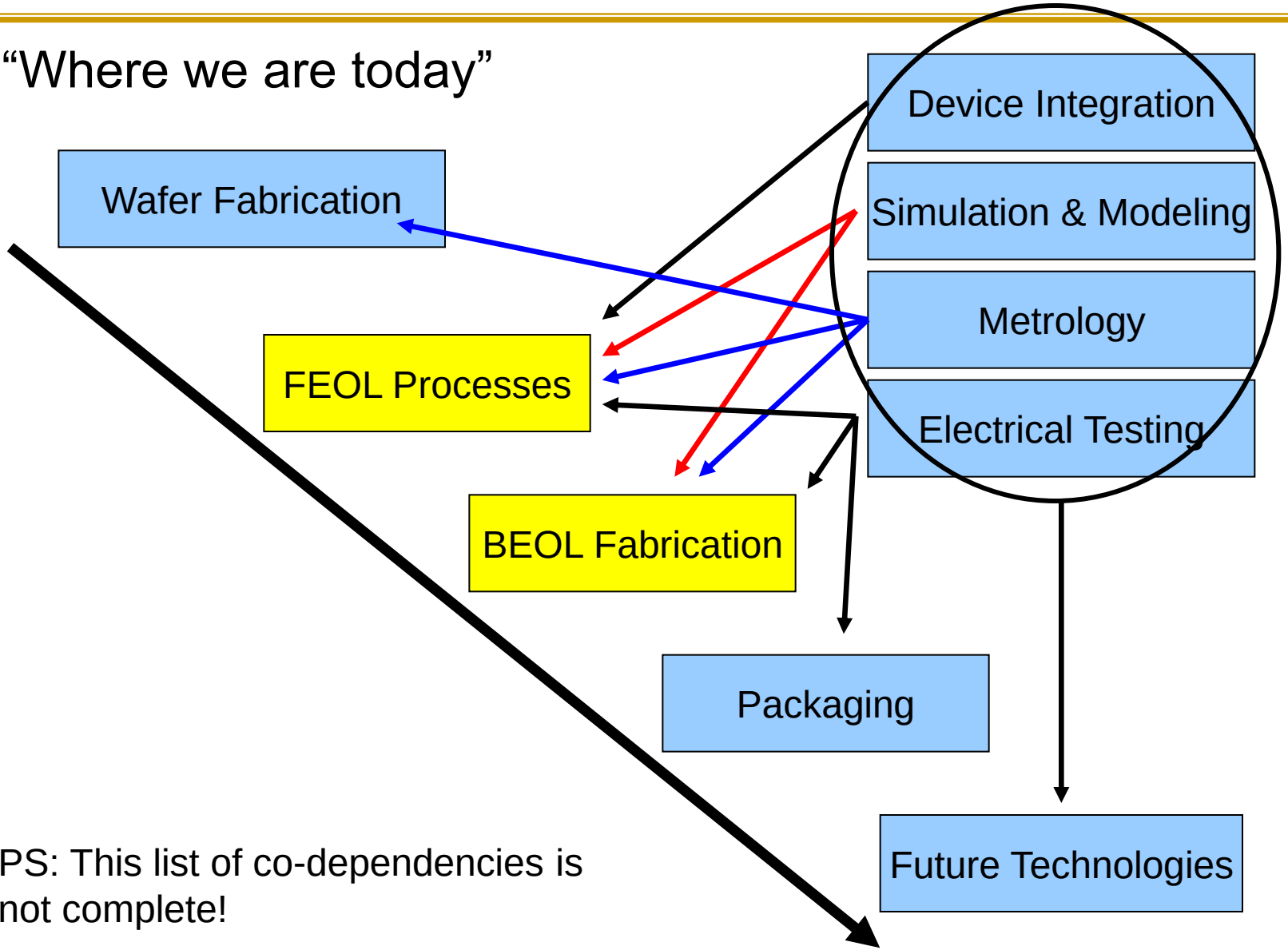
PS: For a short video of the wafer production process see:
http://www.siltronic.com/int/en/press/film/film-overview.jsp

Recap Silicon Epitaxy

- Definition and Terminology
- Chemical Vapor Deposition (CVD) / Vapor Phase Epitaxy (VPE)
    - Grove Model: Mass-transport vs. Surface Reaction Limited Regime
    - Reactors
    - Chemistry
- Reactor Types
- Applications

Lecture 3: Wafer Clean and Wet Processing

"Where we are today"



PS: This list of co-dependencies is not complete!

Lecture 3: Outline

Part 1

- Clean Rooms
- Wafer Cleaning
- Gettering

Part 2

- Silicon Run 1

Introduction

ITRS Roadmap: Defining the term “clean”

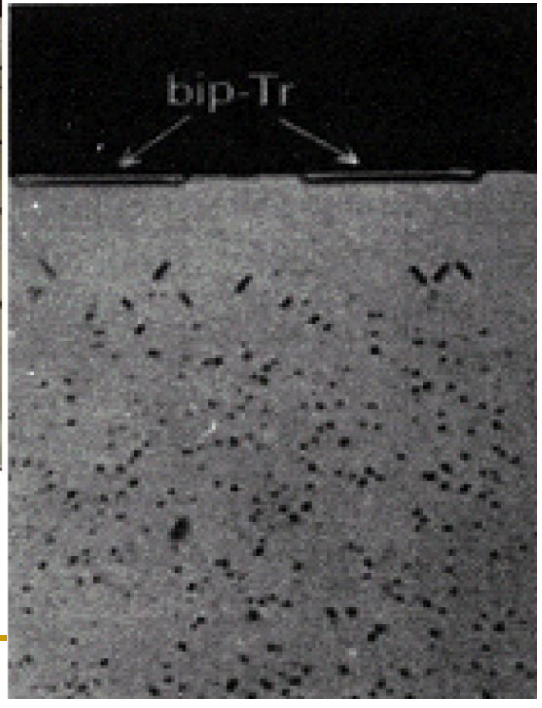
Year of 1st DRAM Shipment	1997	1999	2003	2006	2009	2012
Minimum Feature Size	250nm	180nm	130nm	100nm	70nm	50nm
Wafer Diameter (mm)	200	300	300	300	450	450
DRAM Bits/Chip	256M	1G	4G	16G	64G	256G
DRAM Chip Size (mm^2)	280	400	560	790	1120	1580
Microprocessor Transistors/chip	11M	21M	76M	200M	520M	1.40B
Critical Defect Size	**125nm**	**90nm**	**65nm**	**50nm**	**35nm**	**25nm**
Starting Wafer Total LLS (cm^{-2})	**0.60**	**0.29**	**0.14**	**0.06**	**0.03**	**0.015**
DRAM GOI Defect Density (cm^{-2})	**0.06**	**0.03**	**0.014**	**0.006**	**0.003**	**0.001**
Logic GOI Defect Density (cm^{-2})	**0.15**	**0.15**	**0.08**	**0.05**	**0.04**	**0.03**
Starting Wafer Total Bulk Fe (cm^{-3})	**$3x10^{10}$**	**$1x10^{10}$**	**Under $1x10^{10}$**	**Under $1x10^{10}$**	**Under $1x10^{10}$**	**Under $1x10^{10}$**
Metals onWafer Surface After Cleaning (cm^{-2})	**$5x10^{9}$**	**$4x10^{9}$**	**$2x10^{9}$**	**$1x10^{9}$**	**$< 10^{9}$**	**$< 10^{9}$**
Starting Material Recombination Lifetime (µsec)	**≥ 300**	**≥ 325**	**≥ 325**	**≥ 325**	**≥ 450**	**≥ 450**

Introduction: “Dirt is a natural part of life.”

Modern IC factories employ a three tiered approach to controlling unwanted impurities:

Three tiered approach

1. **Clean Factories (Clean Room)**
2. **Wafer Cleaning**
3. **Gettering**



Factory environment is cleaned by:

- ✓HEPA filters and recirculation for the air.
- ✓“Bunny suits” for workers.
- ✓Filtration of chemicals and gases.
- ✓Manufacturing protocols.

(Photo courtesy of Stanford Nanofabrication Facility.)

HEPA:
High
Efficiency
Particulate
Air

1. Air cleaning

From Intel Museum

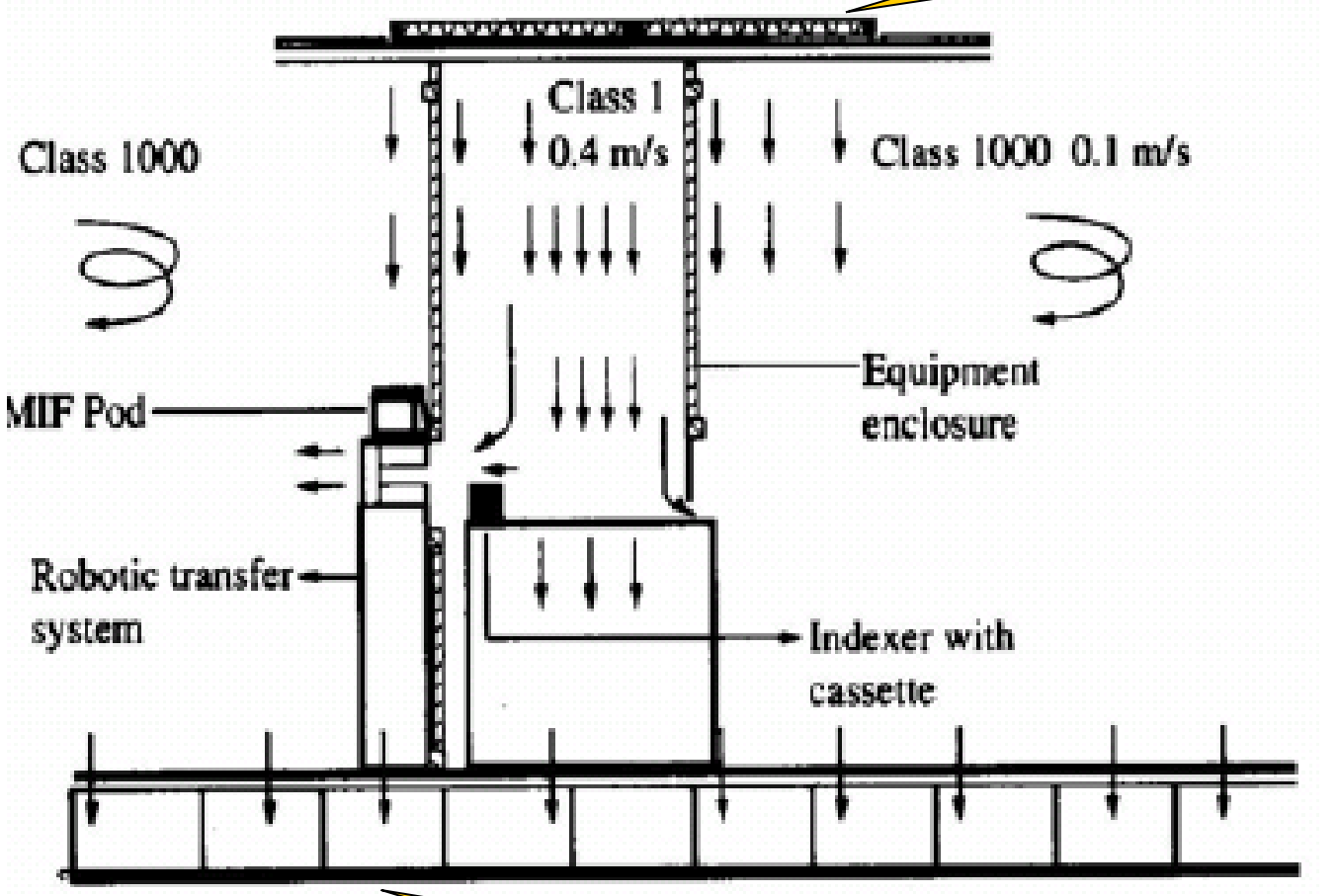
Particle Diameter (um)				
Class	**0.1**	**0.3**	**0.5**	**5.0**
1	35	3	1	
10	350	30	10	
100		300	100	
1,000			1,000	7
10,000			10,000	70
100,000			100,000	700

Electrum Laboratory

ISO Class 5 (Cleanroom Class 100) in APL Litho Room

ISO 14644-1	particles/m^3	areas
ISO class 6: size 0.5 um	35 200	APL, ATP, Hybridisering and Gul 1
ISO class 7: size 0.5 um	352 000	Main cleanroom
ISO class 8: size 0.5 um	3 520 000	Wet chemistry and post-processing

ISO Class 6 = Class 1000



HEPA Filter

Thin Porous Sheets (ultrafine glass fibers): Large particles are trapped by filters and small particles are adsorbed by electrostatics

Recirculation

20～22°C
40～46％RH

Exhaust

Unwanted impurities must be kept below the ppm or ppb range
Critical (Fatal) Defect (Particle) Size = 1/2 Minimum Feature Size

ITRS Feature Year	2007	2010	2013	2016	2020
Minimum Feature Size（nm）	65	45	32	22	14

Three tiered approach
- ✓clean room
- ✓wafer cleaning
- ✓gettering

Particle
Organics: Oil,Photoresist
Metal/Alkali ions
Native oxide

Lecture 3: Outline

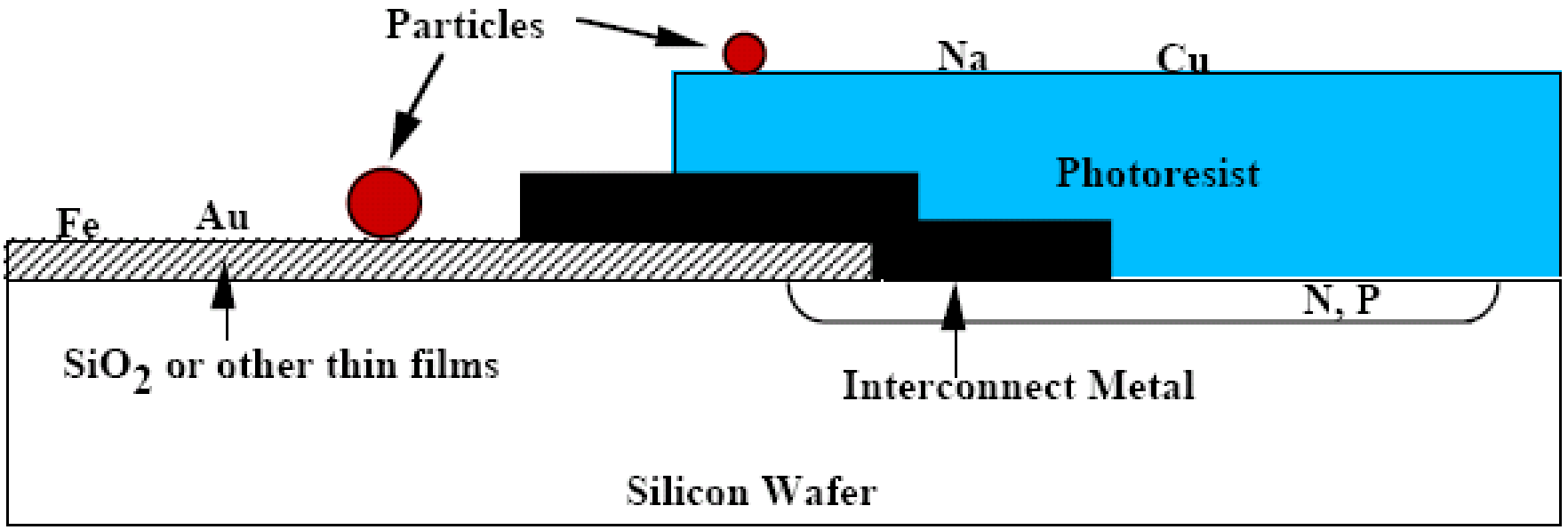
Part 1

- Clean Rooms
- Wafer Cleaning
  - Contamination Sources
  - Cleaning Methods
- Gettering

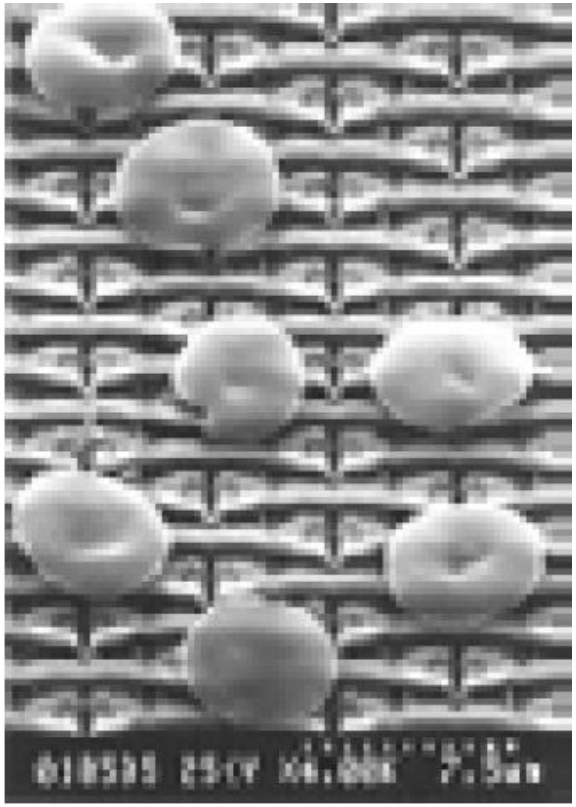
Part 2

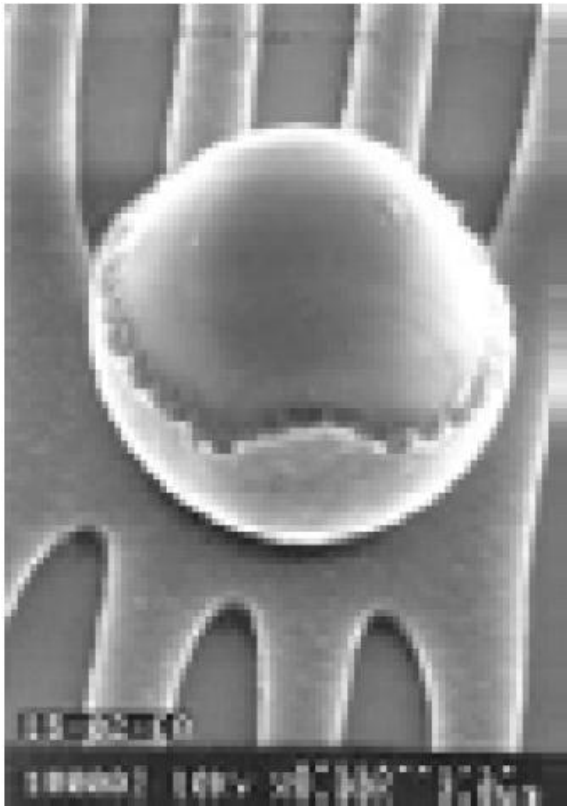
- Silicon Run 1

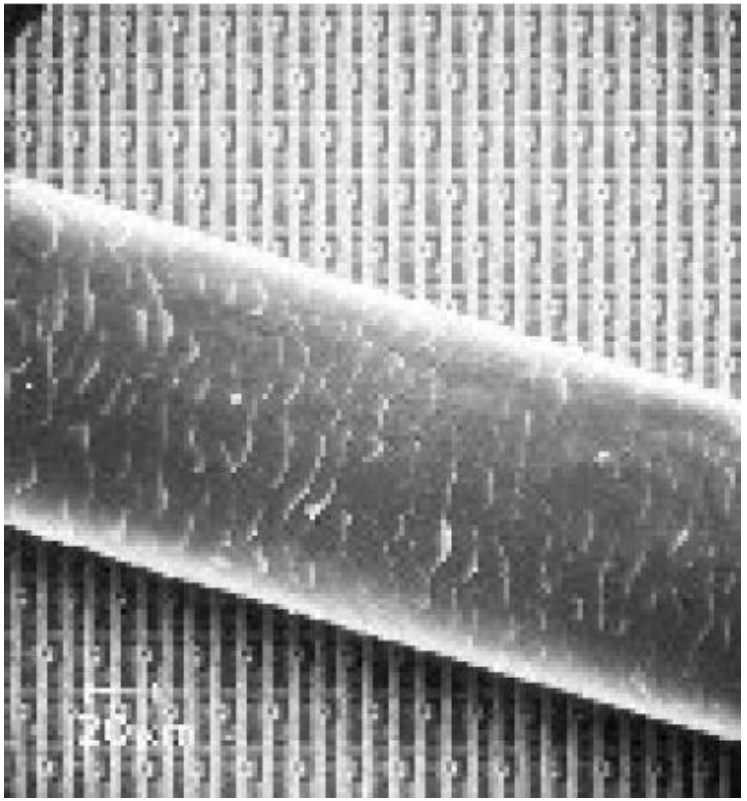
Wafer Cleaning: If a Clean Room is not enough



Contaminants may consist of particles, organic films (photoresist), heavy metals or alkali ions.





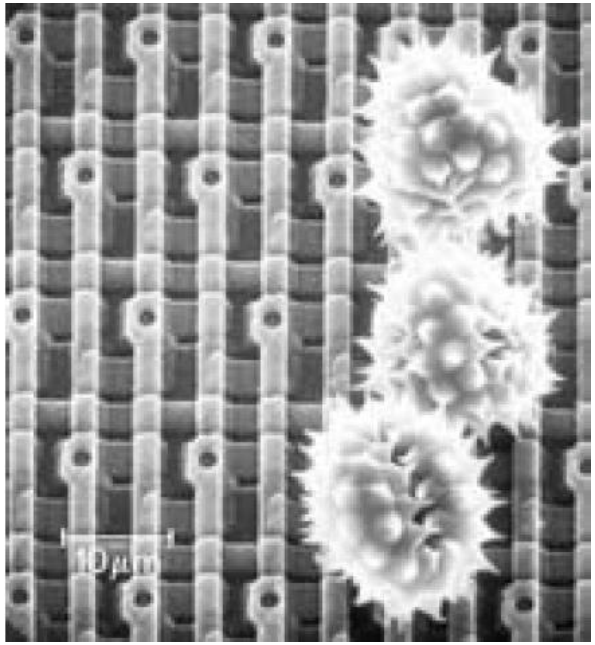


Various particles deposited on chips

Particles might deposit on silicon wafers and cause defects

Source:

- ✓ **Air** — **Super-clean air**
- ✓ **People** — **Air showers, "bunny suits" face masks, gloves; Robots**
- ✓ **Machines** — **Specifically designed**
- ✓ **Chemicals** — **Specifically chosen**



Particle concentration in ULSI chemicals (/ml)

	>0.2mm	>0.5mm
NH_4OH	130-240	15-30
H_2O_2	20-100	5-20
HF	0-1	0
HCl	2-7	1-2
H_2SO_4	180-1150	10-80

Example for a metal organic precursor.

Trimethyl-aluminum.

Specifications

(Electronic Grade TMA)

Metals (all values in ppm)

Ag	<0.4	As	<0.5
Au	<0.5	B	<0.4
Ba	<0.1	Be	<0.02
Bi	<0.5	Cd	<0.02
Ca	<0.2	Co	<0.4
Cr	<0.4	Cu	<0.2
Fe	<0.1	Ge	<0.5
Hg	<0.5	I	<2.0
La	<0.4	Li	<0.4
Mg	<0.02	Mn	<0.03
Mo	<0.5	Na	<1.0
Nb	<0.5	Ni	<0.5
P	<0.5	Pb	<2.0
Pd	<0.5	Pt	<0.5
Rh	<0.5	S	<2.0
Sb	<1.0	Se	<1.0
Si	<2.0	Sn	<2.0
Sr	<0.1	Tb	<0.5
Te	<2.0	Ti	<0.2
V	<0.5	W	<0.5
Y	<0.02	Zn	<0.2

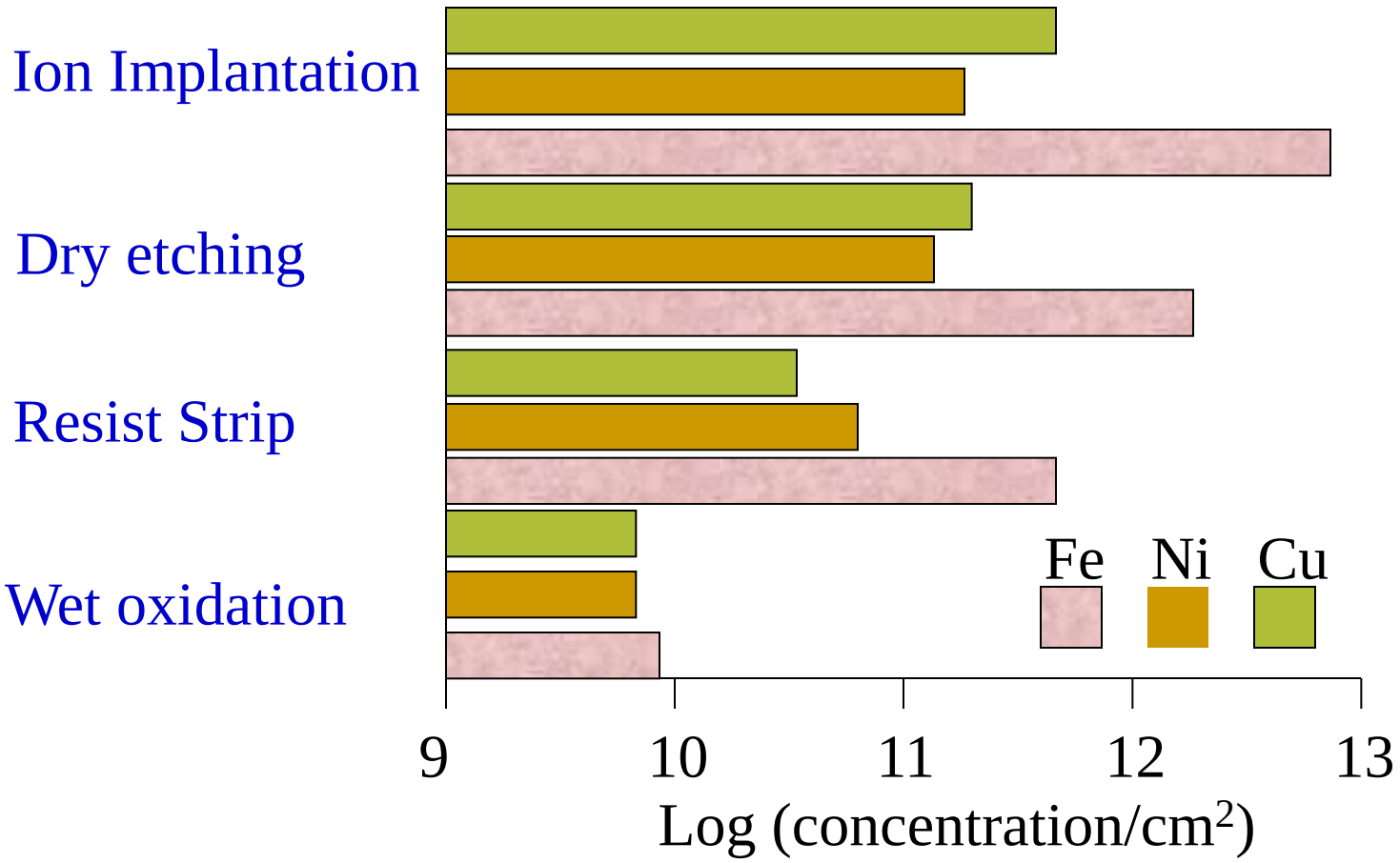
Metal Contamination

- **Source: Chemicals, Processes such as Ion implantation, Reactive Ion etching, etc.**
  - **Magnitude： 10^{10} atom/cm^2**

Fe, Cu, Ni,
Cr, W, Ti…
Na, K, Li…

- **Effects：**
  - ✓ **Cause defects in interfaces, influence device performance and reduce product yield**
  - ✓ **Increase leakage current of p-n junction, decrease lifetime of minority carriers**

Metal contamination from different processes



Organic Contaminations

- **Source：**
  - Ambient organic vapors
  - Storage containers
  - Photoresist residues
- **Removal methods： Strong oxidation**
  - — Ozone dry
  - — Piranha： H_2SO_4-H_2O_2
  - — Ozonized ultrapure water

Native Oxide

- Rapid growth in air or water
- Problems
  - ✓ Increase contact resistance
  - ✓ Difficult to achieve selective CVD or epitaxy
  - ✓ Become sources of metal impurities
  - ✓ Difficult to grow metal silicides
- Clean Process： $HF + H_2O$（ca. 1: 50）

Harm of the unwanted impurity

All components and interconnects in ICs are small → contaminations by dust and metals during manufacturing likely lead to malfunctioning devices or circuits through short or open defects

About 75% of the yield loss in a modern silicon IC manufacturing plant is due directly to defects caused by particles on the wafer.

Example 1. For an IC manufacturing plant, its output is 1000 wafer/week × 100 chip/wafer and the chip price is \$50/chip. The plant is breakeven if the product **yield** is 50%. In order for an annual profit of \$10,000,000, the product yield should increase by

$$\frac{\$1\times10^{7}}{1000\times100\times\$50\times52}=3.8\%$$

Annual throughput
=Annual expense
=1000×100×52×\$50
=\$260,000,000

Increasing the product yield by 3.8%, gives rise to the annual profit of 10 million dollars!

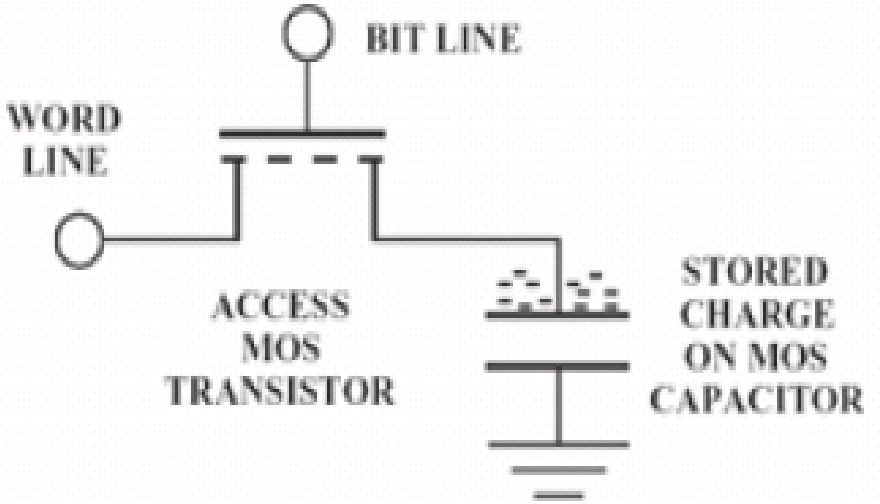
Harm of the unwanted impurity

Example 2. Effects of alkali ions on MOS threshold voltage

$$V_{th} = V_{FB} + 2\Phi_f + \frac{\sqrt{2\varepsilon_s q N_A (2\Phi_f)}}{C_{ox}} + \frac{qQ_M}{C_{ox}}$$

If t_{ox} = 10 nm, when $Q_M = 6.5 \times 10^{11}$ cm^{-2} (≅10 ppm), ΔV_{th} = ?? V

Example 3. Request of MOS DRAM refresh time on trap density N_t



$$\tau_R = \frac{1}{\sigma v_{th} N_t}$$

Typically,

σ = 10^{-15} cm^2, v_{th} = 10^{-7} cm/s

So τ_R = 100 μs requires

$N_t \cong 10^{12}$ cm^{-3} =0.02 ppb !!

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Part 1

- Clean Rooms
- Wafer Cleaning
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Part 2

- Silicon Run 1

Wafer Cleaning: Removing Organics

Two methods to remove Organics/ Photoresists

Piranha（SPM：sulfuric/peroxide mixture）
H_2SO_4(98%):H_2O_2(30%)=2:1~4:1
Oxidize photoresist into CO_2＋H_2O
(applicable to almost all organics)

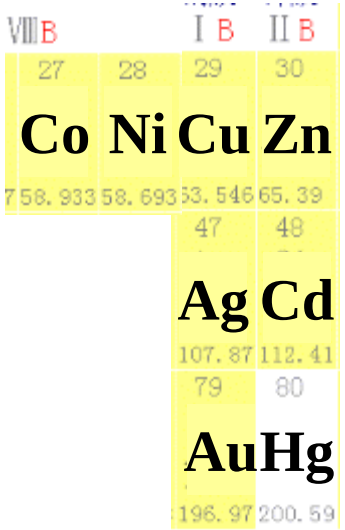
Metal

Oxygen Plasma Dry Etching:
Oxidize photoresist into gaseous CO_2＋H_2O
(applicable to most polymer films)

Note: High-temperature process will drive contaminant into silicon wafer or thin films
Front-end (FEOL) cleaning is crucially important

Wafer Cleaning: Standard Clean 1

RCA——Standard Cleaning



SC-1（APM，Ammonia Peroxide Mixture）：

$NH_4OH(28\%):H_2O_2(30\%):DIH_2O=1:1:5$～1:2:7

70～80°C, 10min **Basic (pH>7)**

-> DIH_2O = De-ionized water

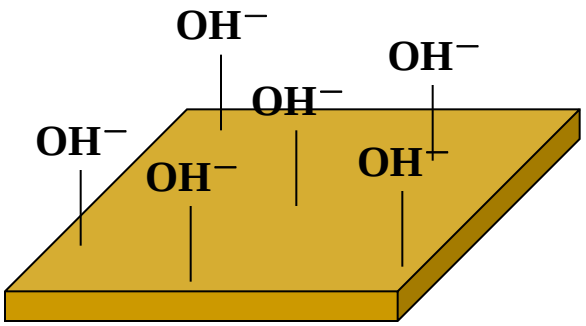
✓Oxidize organic films

✓Complex metals

✓Dissolve slowly native oxide and reoxidize wafer

— help to dislodge particles

✓NH_4OH etches silicon



RCA clean is "standard process" used to remove organics, heavy metals and alkali ions.

Wafer Cleaning: Standard Clean 2

RCA——Standard Cleaning

SC-2:

$HCl(73\%):H_2O_2(30\%):DIH_2O=1:1:6\sim1:2:8$

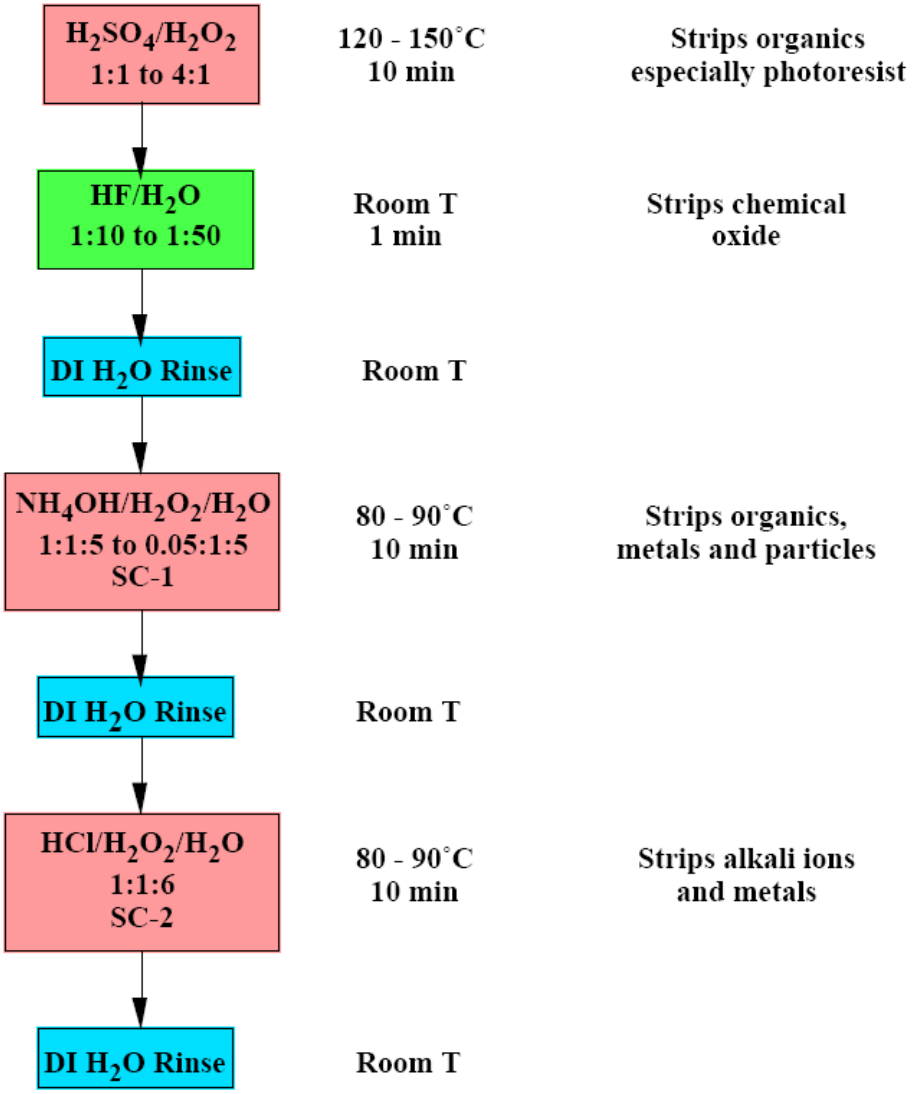
70～80°C, 10min **Acid (pH<7)**

- ✓**Remove alkali ions and cations like Al^{3+}, $Fe^{3+}$and Mg^{2+} that form NH_4OH-insoluble hydroxides in SC-1 solution**
- ✓**Complete the removal of metallic contaminates such as Au**

Combination between RCA and ultrasonic agitation (20～50kHz or around 1MHz) is quite effective for particle removal.

The sound waves parallel to the silicon wafer infiltrate particles. Afterwards, solution can diffuse into the wafer surface and the particles become completely soaked and then suspended freely in the solution.

• RCA clean is “standard process” used to remove organics, heavy metals and alkali ions.



Other Advanced Wet Cleaning Technology, **e.g.** Ohmi

From IMEC (Interuniversity Microelectronic Center)

(1) $H_2O + O_3$ (<1 ppb)
Remove Organics

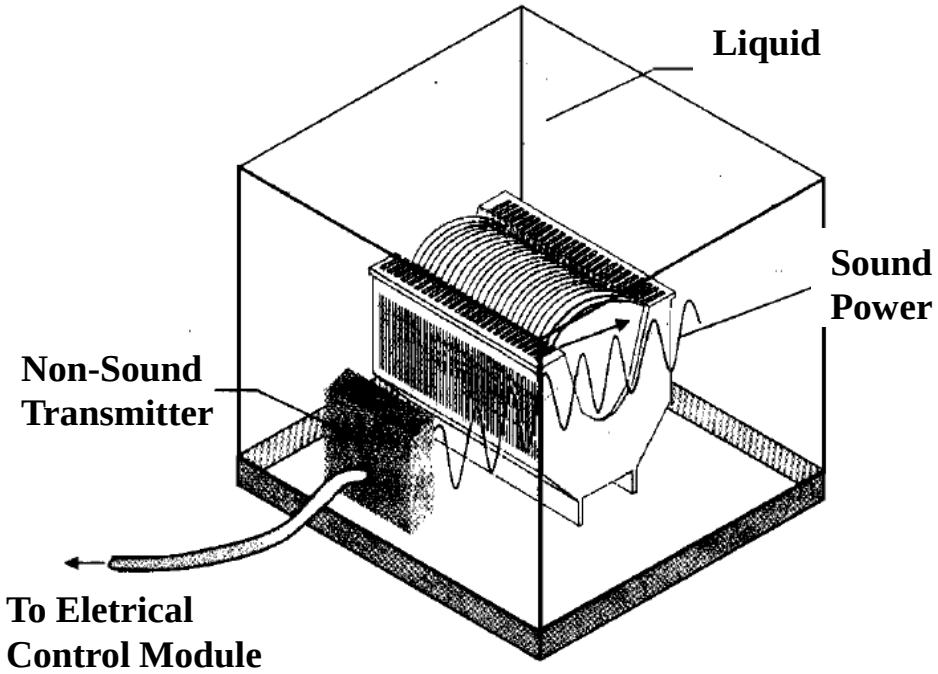
(2) $NH_4OH + H_2O_2 + H_2O$ (0.05:1:5)
Remove Particle, Organics and Metals

(3) HF (0.5%) +H_2O_2 (10%)
Remove Native Oxide and Metals

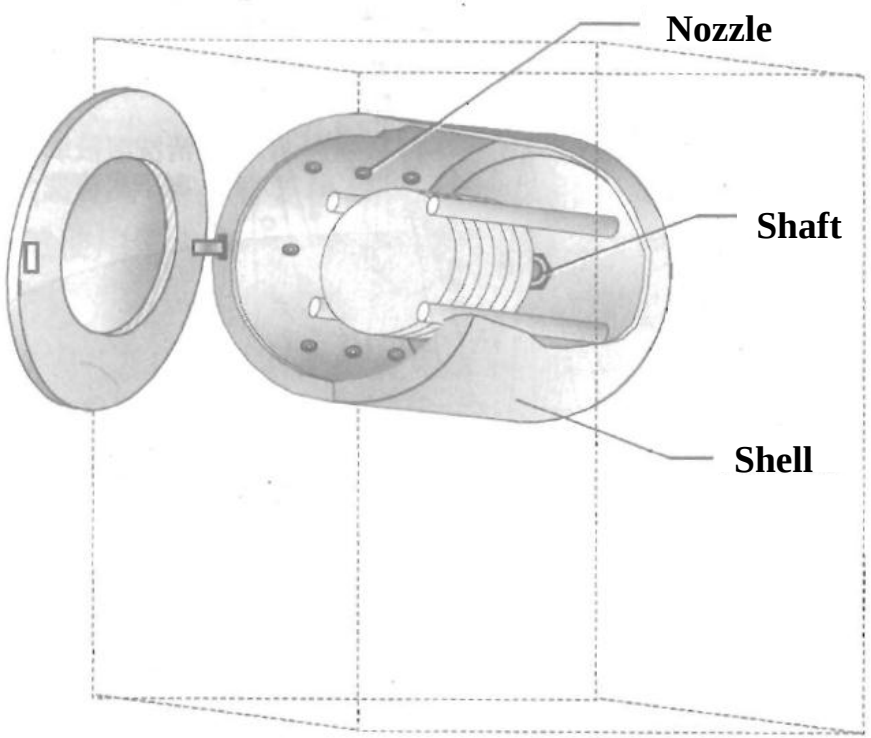
(4) DI H_2O cleaning（>18MΩ-cm)

Cleaning Equipment

Ultrasonic Cleaning



Spray Cleaning



Robot-assisted automatic cleaning station

Container and Carrier Cleaning

✓SC1/SPM/SC2

– Quartz or Teflon container

✓HF

– Prefer Teflon. Other colorless plastic containers are also viable.

✓Silicon wafer carrier

– Only Teflon or Quartz carriers can be used

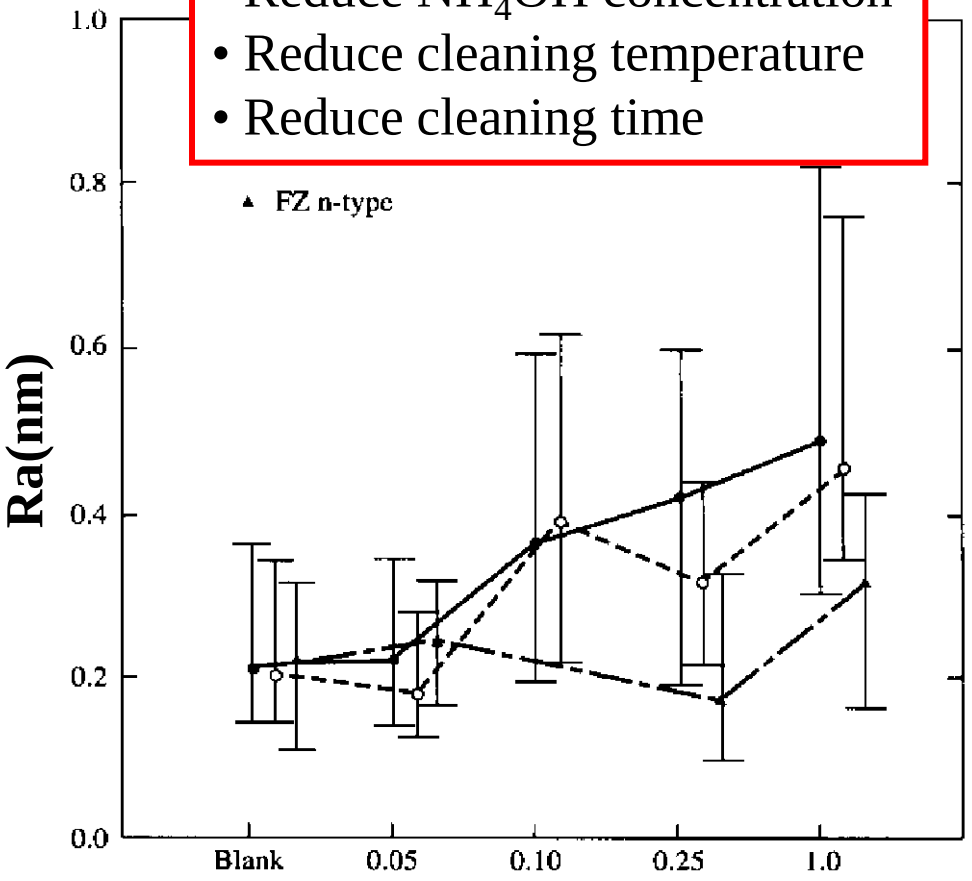
Problems in Wet Cleaning（1）

Surface Roughness: Cleaning agents and metal contaminants may etch silicon wafer and result in micro-roughness on the surface. High-concentration NH_4OH in SC-1 may etch and damage the silicon surface.

How to reduce micro-roughness
- Reduce NH_4OH concentration
- Reduce cleaning temperature
- Reduce cleaning time

Reduce the carrier mobility in the channels

Have devastating effects on the quality and breakdown voltage of thermally-grown gate oxide.



Mixing ratio of NH_4OH(A) in $NH_4OH+H_2O_2+H_2O$ solution (A:1:5, A<1)

Problem in Wet Cleaning（2）

- ✓Introduce particles
- ✓Difficult to Dry
- ✓Cost
- ✓Chemical waste disposal
- ✓Incompatible with advanced integrated technology

Dry Cleaning Technology

- Gas Chemistry. Usually activation energy is needed to enhance chemical reactions at low temperatures.
- The required energy may come from plasma, ion beam, shortwave radiation and heating. The energy is used to clean silicon wafers, but must be prevented from damaging them.

  - ✓HF/H_2O Gas Cleaning
  - ✓Ultraviolet Ozone Cleaning（UVOC）
  - ✓H_2/Ar Plasma Cleaning
  - ✓Heat Cleaning

Lecture 3: Outline

Part 1

- Clean Rooms
- Wafer Cleaning
- Gettering

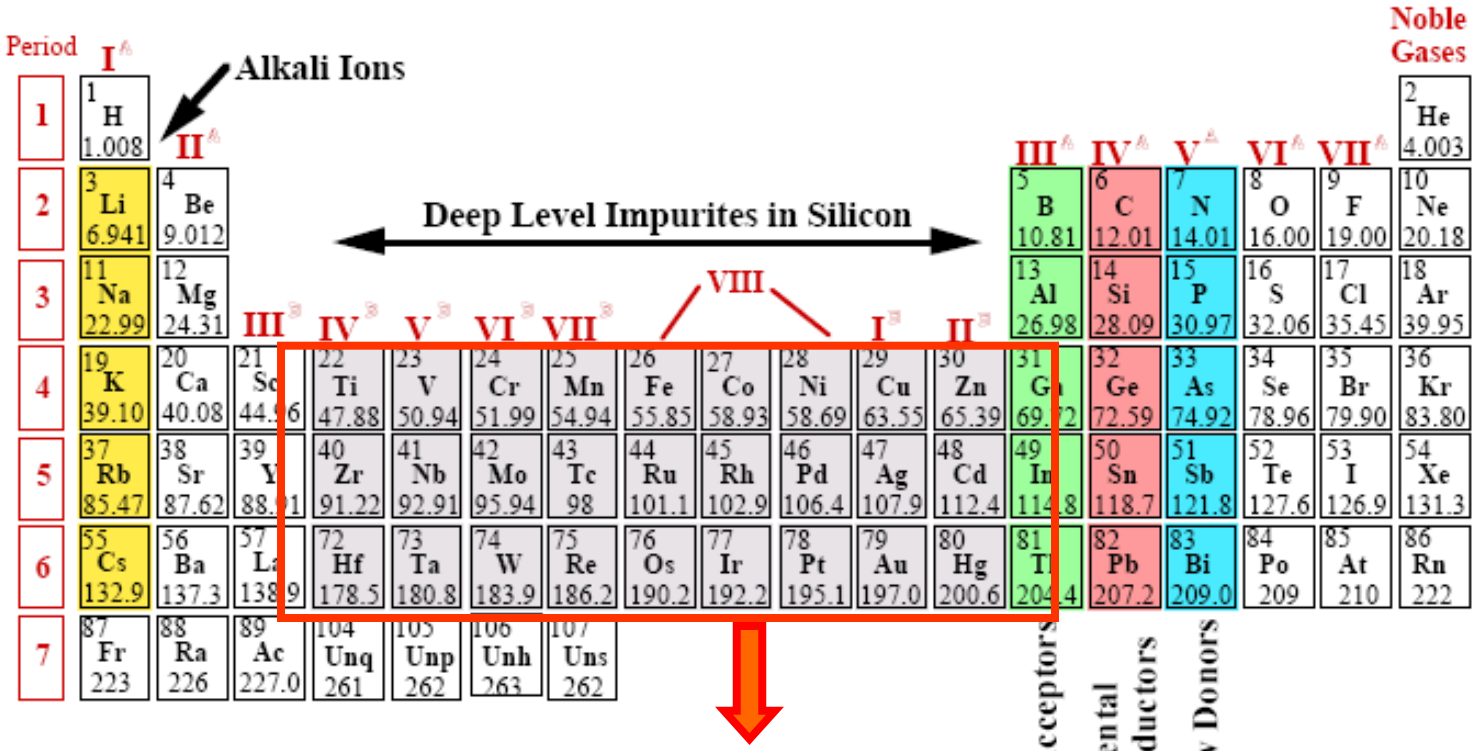
Part 2

- Silicon Run 1

Gettering

Level 3 Contamination Reduction: Gettering

• Gettering is used to remove metal ions and alkali ionsfrom device active regions.



These elements tend to have very high diffusivities and be easily captured in regions with either mechanical defects or chemical traps.

Gettering

Capture defects at locations far away from the device region.

Damaged region will act as "sink" for unwanted elements.

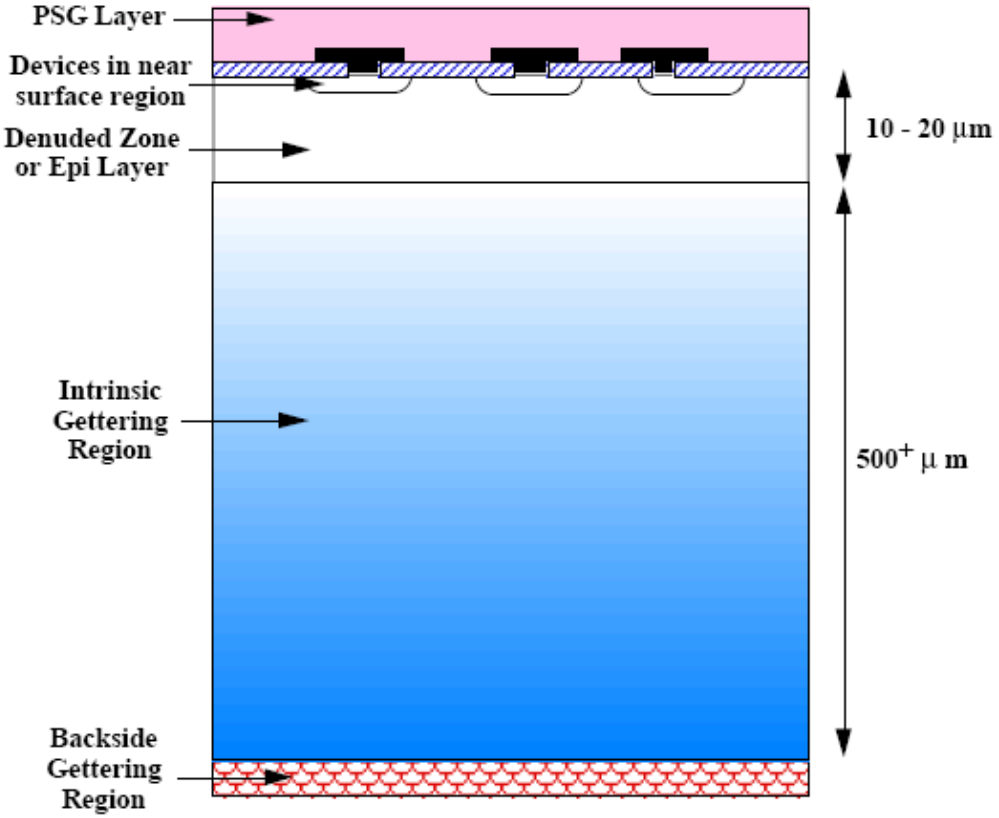
Metals diffuse as interstitials (>> diffusivity than dopants)

Metals need defects to become

- Dislocations
- Stacking faults
- Grain boundaries
- Precipitates (e.g. O_2)

PSG captures alkali ions

(Phosphosilicate Glas)



General Stategy

1. Free impurities
2. Diffuse to gettering site
3. Trap at gettering site

Gettering

Release → Mobile, increase diffusivity.
Substitutional atom → Interstitial atom

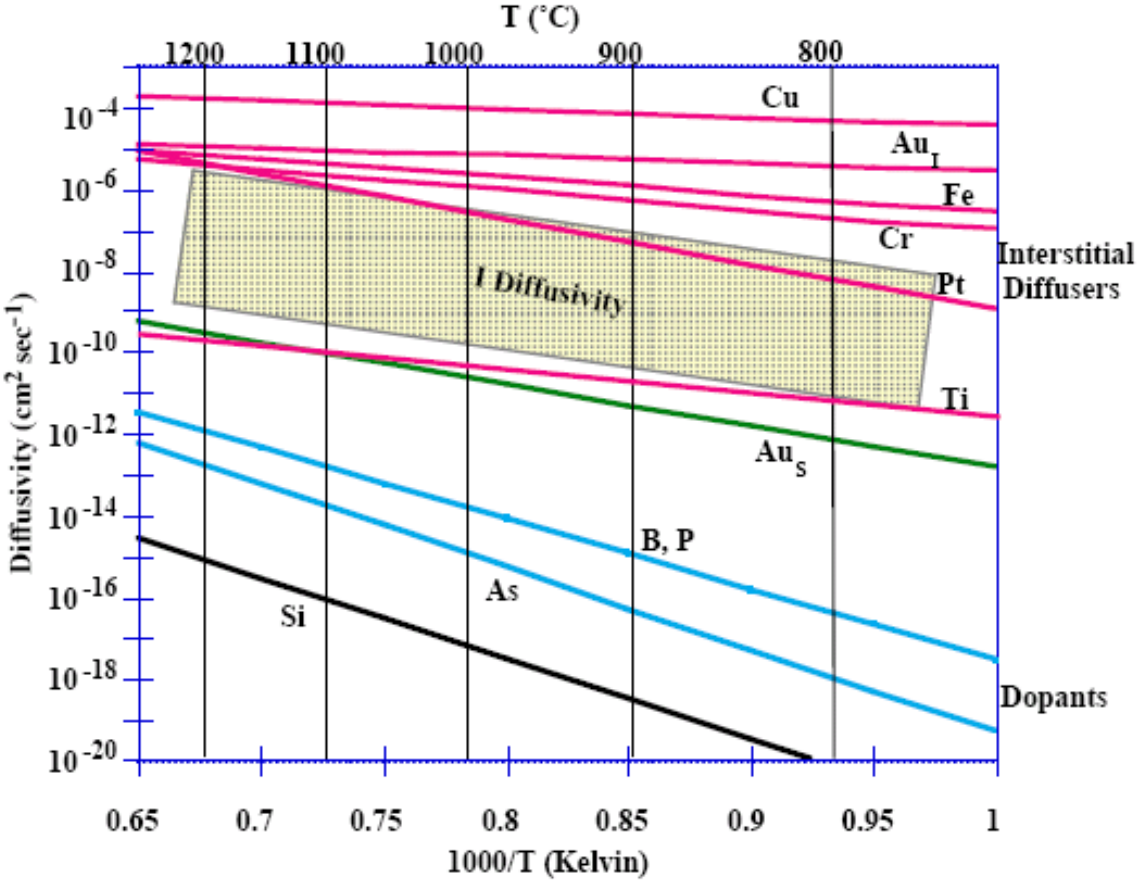
$Au_s + I \Leftrightarrow Au_I$ **"kick-out" mechanism**
$Au_s \Leftrightarrow Au_I + V$ **"dissociative" mechanism**

Introduction of a large number of interstitial silicon atoms may convert substitutional atoms, such as Au and Pt, to interstitial atoms and hence increase their diffusivity.

Method {
- **High-concentration phosphorous diffusion**
- **Ion implantation damage**
- **SiO_2 precipitates**

Gettering: Metals

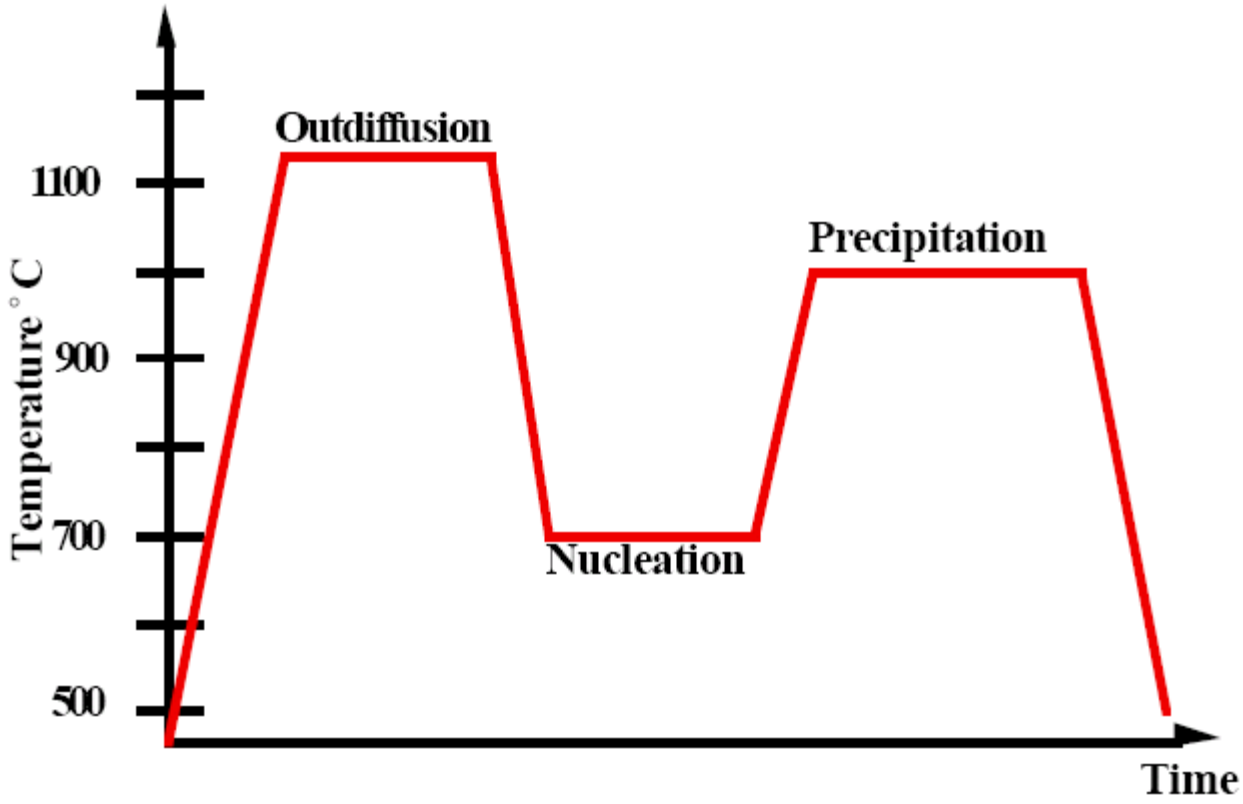
- **Heavy metal gettering relies on:**
  - Metals diffusing very rapidly in silicon
  - Metals segregating to “trap” sites.



Gettering: Metals

•"Trap" sites can be created by SiO_2 precipitates (intrinsic gettering), or by backside damage (extrinsic gettering).

• In intrinsic gettering, CZ silicon is used and SiO_2 precipitates are formed in the wafer bulk through temperature cycling at the start of the process.



Gettering

✓**PSG —— Form stable complexes that bind alkali ions**

At temperatures above room temperature, alkali ions will easily diffuse to and be trapped by PSG layers

✓**Clean Processing + Si_3N_4 cap layer**

—— Barriers to indiffusion of alkali ions

Metal ions Gettering

✓**Intrinsic Gettering —— Drive oxygen atoms in silicon from the near surface region, up to 10~20 μm in depth, into the bulk and reduce the oxygen concentration within the near surface region to below 10 ppm. The SiO_2 precipitates in the silicon bulk create the trap sites for gettering.**

✓**Extrinsic Gettering —— Create defects or traps sites for gettering by producing damage or depositing poly-silicon films on the backside. Subsequent high-temperature processing step will allow metal ions to diffuse to the backside and complete the gettering simultaneously.**

Summary of Key Ideas

Cleaning Necessity

- Devices: Minority carrier lifetime↓, V_T changes, I_{on}↓ I_{off}↑, Gate breakdown voltage ↓, Reliability ↓
- Circuit: Yield↓, Electrical performance↓

3 Levels: Clean room, Wafer cleaning and Gettering

⇩

Cleaning Class
Efficient Cleaning

Contaminations: Particles, Organics, Metals, Native oxide ⟹ **Strong Oxidation**

↳ **HF:DI H_2O**

The bottom line is chip yield. "Bad" die manufactured alongside "good" die. Increasing yield leads to better profitability in manufacturing chips.

Summary of Key Ideas

Wafer Cleaning
Wet Cleaning: Piranha, RCA (SC-1,SC-2), HF:H_2O
Dry Cleaning: Phase Chemistry, Supercritical Fluid

Gettering: Release, Diffusion, Trapping
Alkali ions: PSG, Cleaning processing + Si_3N_4 Cap layers
Other metals: Intrinsic Gettering and Extrinsic Gettering
——High-concentration Silicon interstitials + Defects

SiO_2 Nucleation Growth; Epitaxial Silicon and Thermal Cycling

High-concentration defects on silicon backside; Poly-Silicon Deposition