

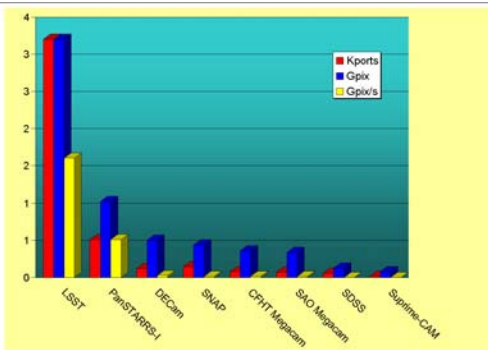
# Large Synoptic Survey Telescope

## LSST Camera Electronics

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The 3.2 Gpixel LSST camera will be read out by means of 189 highly segmented 4K x 4K CCDs. A total of 3024 video channels will be processed by a modular, in-cryostat electronics package based on two custom multichannel analog ASICs now in development. Performance goals of 5 electrons noise, .01% electronic crosstalk, and 80 mW power dissipation per channel are targeted. The focal plane is organized as a set of 12K x 12K sub-mosaics ("rafts") with front end electronics housed in an enclosure falling within the footprint of the CCDs making up the raft. CCD surfaces within a raft are required to be coplanar to within 6.5 microns. The assembly of CCDs, baseplate, electronics boards, and cooling components constitutes a self-contained and testable 144 Mpix imager ("raft tower"), and 21 identical raft towers make up the LSST science focal plane. Electronic, mechanical, and thermal prototypes are now undergoing testing and results will be presented at the meeting.

### Camera Development Comparisons



### The Challenge

- ~3,200 Megapixels
- 6 e rms read noise
- 2 sec read time
- 90k e full well
- Minimize vacuum feedthrough count

### Sensors

- 4k x 4k CCDs with 10u pixels (16 Mp)
- 10u pixels → ~ 40mm x 40mm
- Each sensor divided into 16 x 1MP segments (16 output ports)
- ~150 bond pads / sensor

### Rafts

- 3 x 3 array of sensors
- 144 output ports
- ~ 125mm x 125mm
- Each raft functions as an autonomous camera

### Focal Plane Array

- 21 fully populated rafts
- 4 partially populated "corner" rafts
- ~ 3,200 readout ports
- ~ 40,000 sensor bond pads

### FPA Readout

- Modular by raft
- Fully synchronous
- Divided into two regions
  - Front End → Analog signal processing, clock driver translation, bias distribution
  - Back End → Analog/Digital conversion, single data fiber output
- Master "Timing & Control" card common to all rafts insures synchronicity
- FPA electronics in cryostat to minimize vacuum feedthroughs

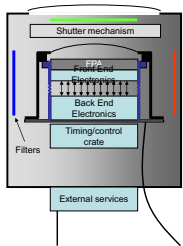
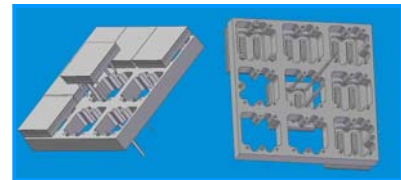
### Electronics packaging and cooling

- Copper core PCBs for heat conduction
- Polyimide PCBs
- Front End Electronics
  - 2x 8 Channel "Dual Slope Integrator" ASIC per sensor
  - Clock driver ASIC (Sensor Control Chip) HV CMOS process
- Back End Electronics
  - 2x 24 channel ADC cards per row of 3 CCDs
  - 6x 24 channel ADC cards per raft

### 16 Segment CCD imagers

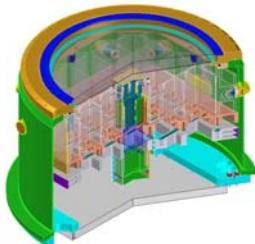


### 9 Sensor Raft Structure



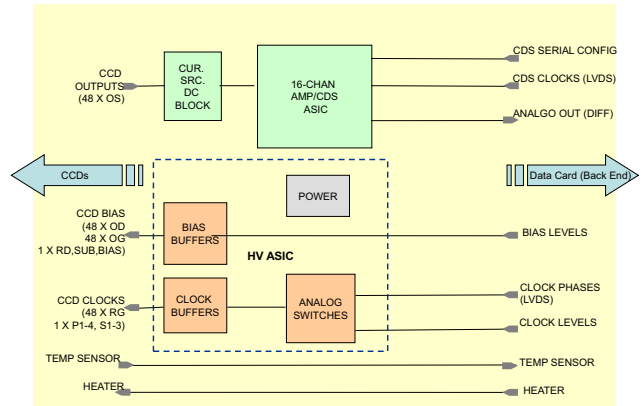
Overall Camera Electronics Distribution showing Front End & Back End Electronics in Cryostat

Cryostat solid model with single raft and electronics



Dwg courtesy M. Nordby, G. Guiffre

### Front End ASIC Functionality



### 24 Ch Back End ADC card

